SONY

Diagonal 12.86 mm (Type 1/1.2) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

IMX485LQJ-C

STARVIS

Description

The IMX485LQJ-C is a diagonal 12.8 mm (Type 1/1.2) CMOS active pixel type solid-state image sensor with a square pixel array and 8.42 M effective pixels. This chip operates with analog 2.9 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-integration time.
(Applications: Surveillance cameras, FA cameras, Industrial cameras)

Features

- ◆ CMOS active pixel type dots
- ◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆ Input frequency: 6 to 27 MHz / 37.125 MHz / 74.25 MHz
- ◆ Number of recommended recording pixels: 3840 (H) × 2160 (V) approx. 8.29M pixel
- ◆ Readout mode
  - All-pixel scan mode
  - Horizontal / Vertical 2/2-line binning mode
  - Window cropping mode
  - Horizontal / Vertical direction - Normal / Inverted readout mode
- ◆ Readout rate
  - Maximum frame rate in
  - All-pixel scan mode: 12 bit: 60 frame/s, 10 bit: 90.1 frame/s
- ◆ High dynamic range (HDR) function
  - Multiple exposure HDR
  - Digital overlap HDR
- ◆ Synchronizing sensors function
- ◆ Variable-speed shutter function (resolution 2H units)
- ◆ 10-bit / 12-bit A/D converter
- ◆ Conversion gain switching (HCG Mode / LCG Mode)
- ◆ CDS / PGA function
  0 dB to 72 dB (step pitch 0.3 dB)
- ◆ Supports I/O
  CSI-2 serial data output (2 Lane / 4 Lane / 8Lane / 4Lane × 2ch) RAW10 / RAW12 output

E19903C03

Device Structure

- ◆ CMOS image sensor
- ◆ Image size
  Diagonal 12.8 mm (Type 1/1.2) approx. 8.40 M pixels, All pixels
- ◆ Total number of pixels
  3864 (H) × 2200 (V) approx.8.50 M pixels
- ◆ Number of effective pixels
  3864 (H) × 2180 (V) approx. 8.42 M pixels
- ◆ Number of active pixels
  3864 (H) × 2176 (V) approx. 8.40 M pixels
- ◆ Number of recommended recording pixels
  3840 (H) × 2160 (V) approx. 8.29 M pixels
- ◆ Unit cell size
  2.9 µm (H) × 2.9 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 20 pixels, rear 0 pixels
- ◆ Dummy
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 0 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog: 2.9 V)	AV_{DD}	-0.3	3.3	V	
Supply voltage (interface: 1.8 V)	OV_{DD}	-0.3	3.3	V	
Supply voltage (digital: 1.2 V)	DV_{DD}	-0.3	2.0	V	
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	85	˚C	
Storage temperature	Tstg	-40	85	˚C	

Application Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog: 2.9 V)	AV_{DD1}	2.80	2.90	3.00	V
Supply voltage (interface: 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (digital: 1.2 V)	DV_{DD1}	1.10	1.20	1.30	V
Performance guarantee temperature	Tspec	-10	—	60	˚C

USE RESTRICTION NOTICE

This USE RESTRICTION NOTICE ("Notice") is for customers who are considering or currently using the image sensor products ("Products") set forth in this specifications book. Sony Semiconductor Solutions Corporation ("SSS") may, at any time, modify this Notice which will be available to you in the latest specifications book for the Products. You should abide by the latest version of this Notice. If a SSS subsidiary or distributor has its own use restriction notice on the Products, such a use restriction notice will additionally apply between you and the subsidiary or distributor. You should consult a sales representative of the subsidiary or distributor of SSS on such a use restriction notice when you consider using the Products.

Use Restrictions

- The Products are intended for incorporation into such general electronic equipment as office products, communication products, measurement products, and home electronics products in accordance with the terms and conditions set forth in this specifications book and otherwise notified by SSS from time to time.
- You should not use the Products for critical applications which may pose a life- or injury-threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. You should consult your sales representative beforehand when you consider using the Products for such critical applications. In addition, you should not use the Products in weapon or military equipment.
- SSS disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

Design for Safety

- SSS is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

Export Control

- If the Products are controlled items under the export control laws or regulations of various countries, approval may be required for the export of the Products under the said laws or regulations. You should be responsible for compliance with the said laws or regulations.

No License Implied

- The technical information shown in this specifications book is for your reference purposes only. The availability of this specifications book shall not be construed as giving any indication that SSS and its licensors will license any intellectual property rights in such information by any implication or otherwise. SSS will not assume responsibility for any problems in connection with your use of such information or for any infringement of third-party rights due to the same. It is therefore your sole legal and financial responsibility to resolve any such problems and infringement.

Governing Law

- This Notice shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this Notice shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

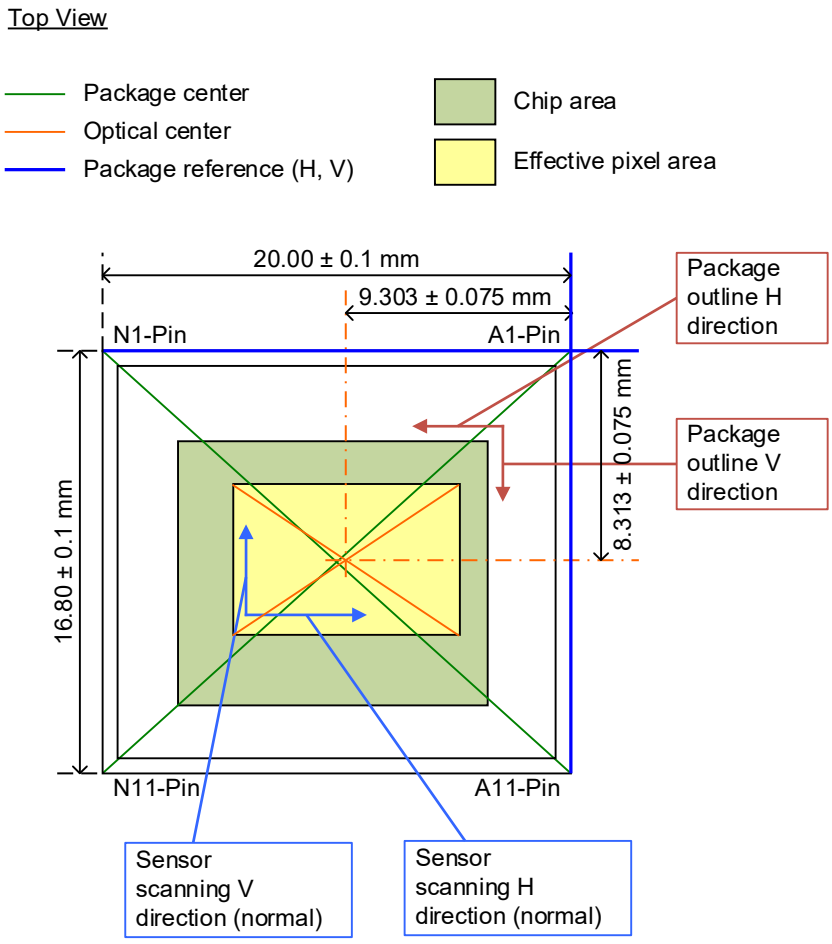
Other Applicable Terms and Conditions

- The terms and conditions in the SSS additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

General-0.0.9

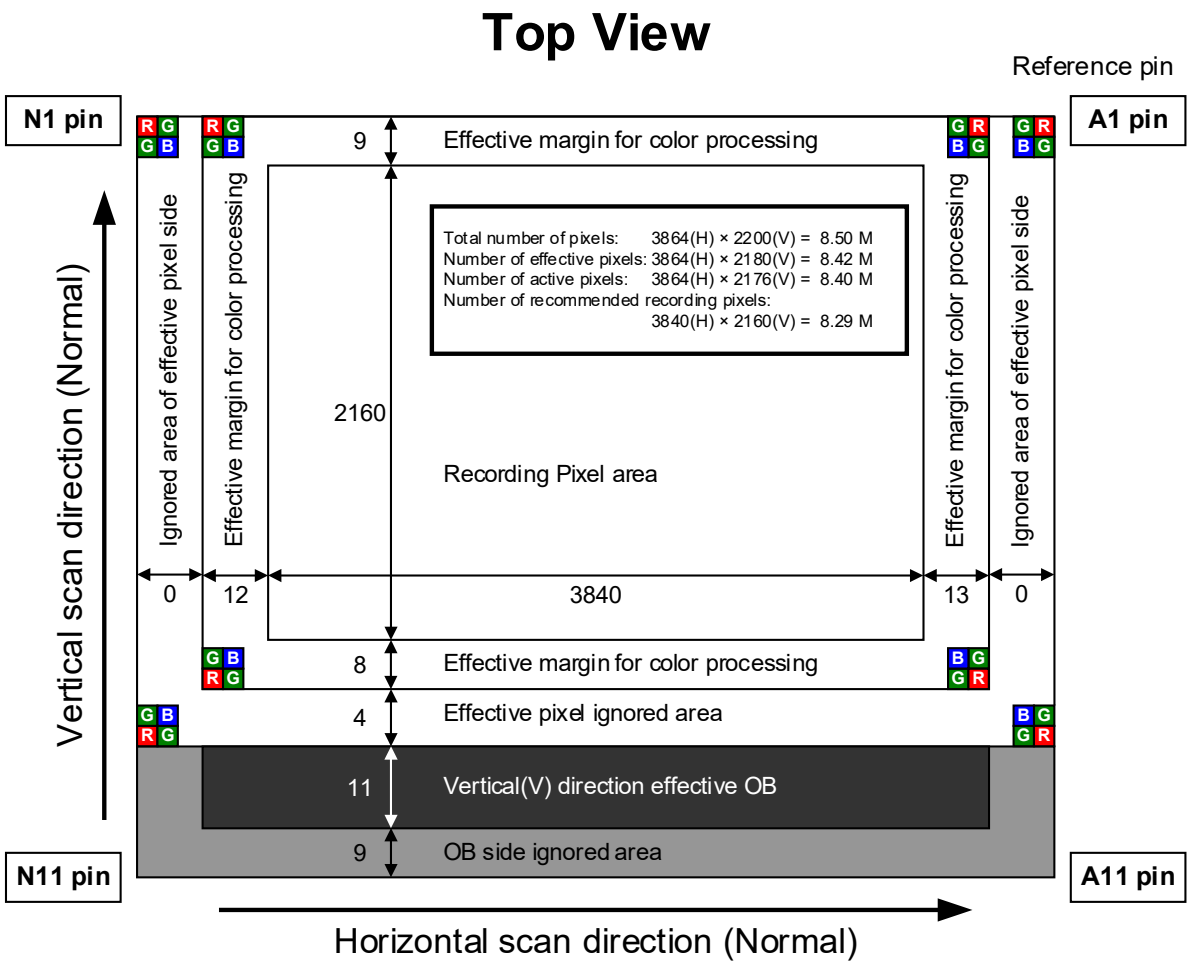
Contents

Optical Center



Optical Center

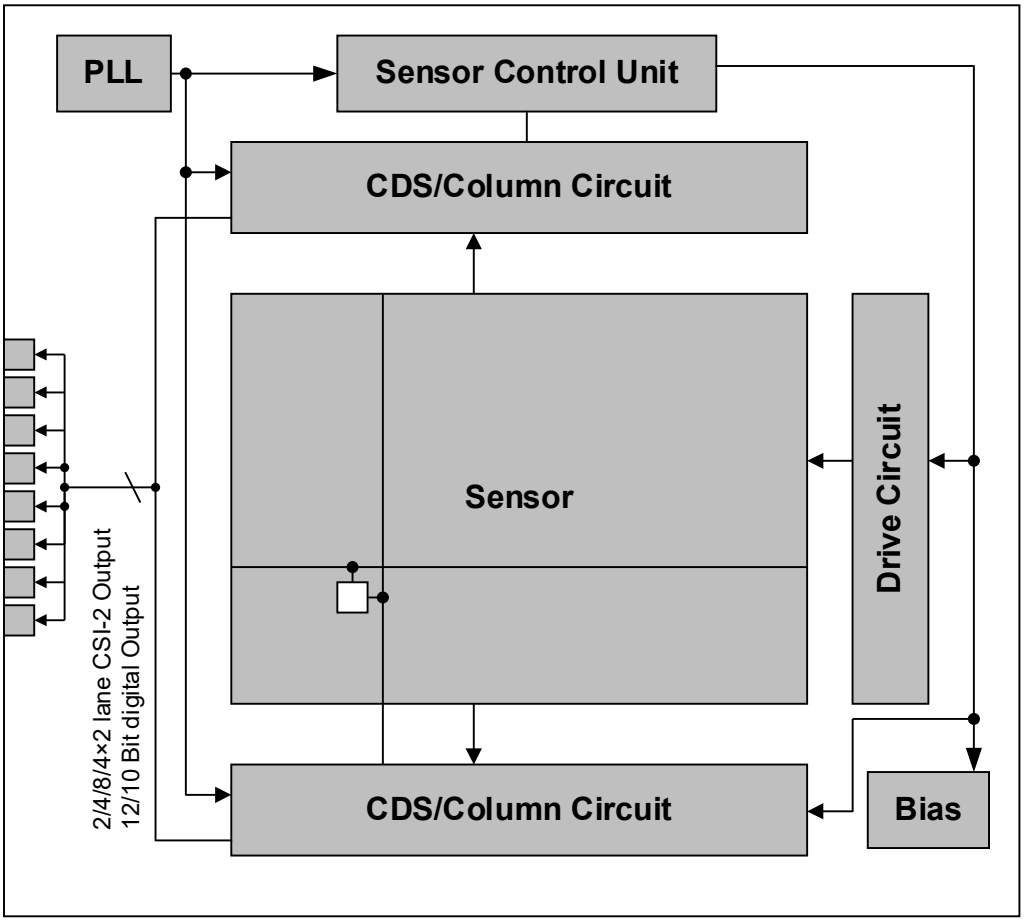
Pixel Arrangement



* Reference pin number is consecutive numbering of package pin array.
See the Pin Configuration for the number of each pin.
The last Effective line and column are not read-out.

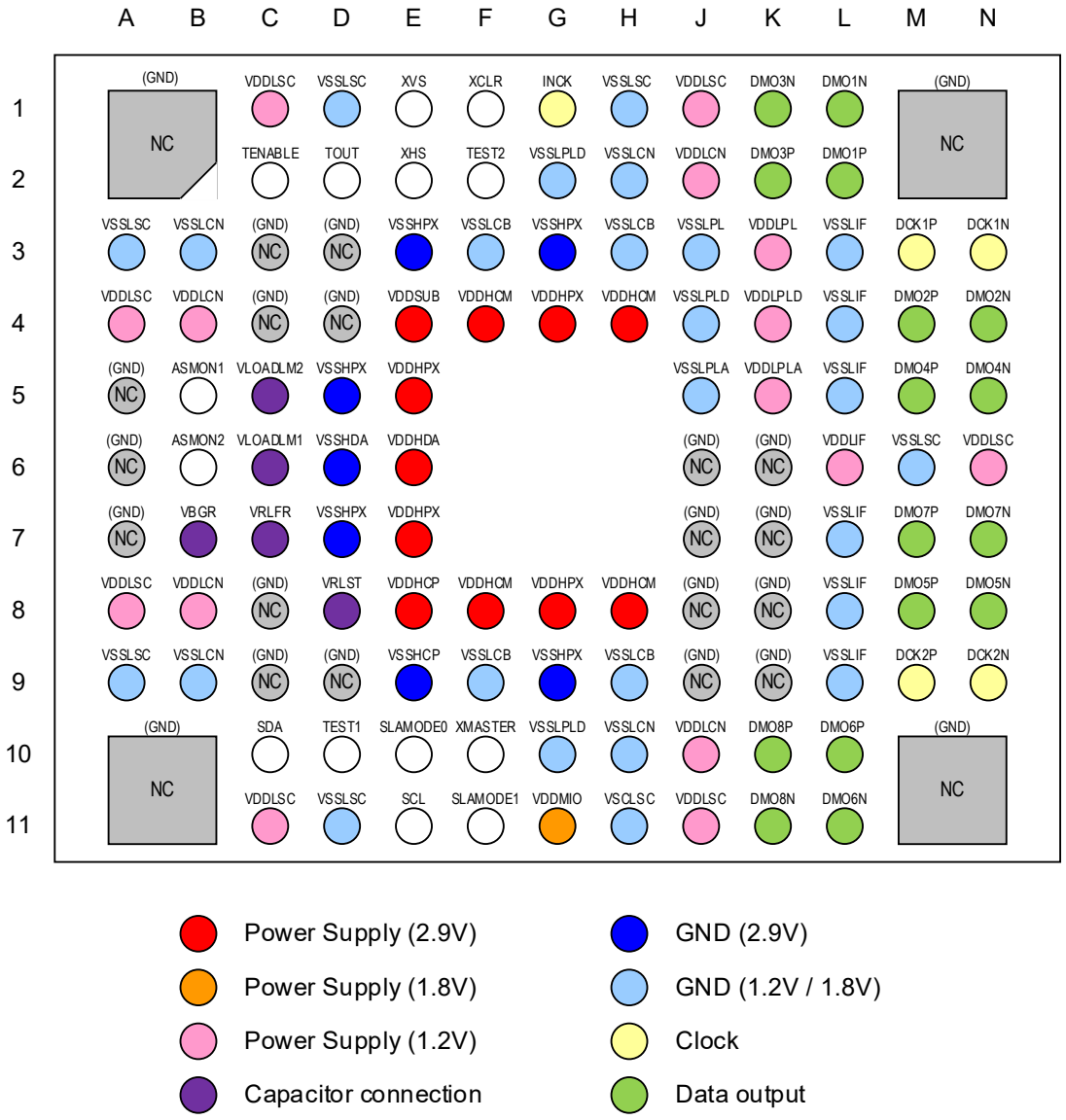
Pixel Arrangement

Block Diagram and Pin Configuration



Block Diagram

Bottom View



*The N.C. pin with (GND) can be connected to GND.

Pin Configuration

Pin Description

No.	Pin No	I/O	Analog / Digital	Symbol	Description
1	A1	—	—	N.C.	GND connectable
2	A3	GND	D	VSSLSC	1.2 V / 1.8 V GND
3	A4	Power	D	VDDLSC	1.2 V power supply
4	A5	—	—	N.C.	GND connection is allowed
5	A6	—	—	N.C.	GND connection is allowed
6	A7	—	—	N.C.	GND connection is allowed
7	A8	Power	D	VDDLSC	1.2 V power supply
8	A9	GND	D	VSSLSC	1.2 V / 1.8 V GND
9	A11	—	—	N.C.	GND connectable
10	B3	GND	D	VSSLCN	1.2 V / 1.8 V GND
11	B4	Power	D	VDDLCN	1.2 V power supply
12	B5	O	A	ASMON1	TEST output pin, OPEN
13	B6	O	A	ASMON2	TEST output pin, OPEN
14	B7	O	A	VBGR	Capacitor connection
15	B8	Power	D	VDDLCN	1.2 V power supply
16	B9	GND	D	VSSLCN	1.2 V / 1.8 V GND
17	C1	Power	D	VDDLSC	1.2 V power supply
18	C2	I	D	TENABLE	Test enable, OPEN
19	C3	—	—	N.C.	GND connectable
20	C4	—	—	N.C.	GND connectable
21	C5	O	A	VLOADLM2	Capacitor connection
22	C6	O	A	VLOADLM1	Capacitor connection
23	C7	O	A	VRLFR	Capacitor connection
24	C8	—	—	N.C.	GND connectable
25	C9	—	—	N.C.	GND connectable
26	C10	I/O	D	SDA	Serial data communication
27	C11	Power	D	VDDLSC	1.2 V power supply
28	D1	GND	D	VSSLSC	1.2 V / 1.8 V GND
29	D2	I/O	D	TOUT	TEST output pin, OPEN
30	D3	—	—	N.C.	GND connectable
31	D4	—	—	N.C.	GND connectable
32	D5	GND	A	VSSHPX	2.9 V GND
33	D6	GND	A	VSSHDA	2.9 V GND
34	D7	GND	A	VSSHPX	2.9 V GND
35	D8	O	A	VRLST	Capacitor connection
36	D9	—	—	N.C.	GND connectable
37	D10	O	D	TEST1	TEST output pin, OPEN
38	D11	GND	D	VSSLSC	1.2 V / 1.8 V GND
39	E1	I/O	D	XVS	Vertical sync signal
40	E2	I/O	D	XHS	Horizontal sync signal
41	E3	GND	A	VSSHPX	2.9 V GND
42	E4	Power	A	VDDSUB	2.9 V power supply
43	E5	Power	A	VDDHPX	2.9 V power supply
44	E6	Power	A	VDDHDA	2.9 V power supply
45	E7	Power	A	VDDHPX	2.9 V power supply
46	E8	Power	A	VDDHCP	2.9 V power supply

No.	Pin No	I/O	Analog / Digital	Symbol	Description
47	E9	GND	A	VSSHCP	2.9 V GND
48	E10	I	D	SLAMODE0	Reference pin, Select slave address
49	E11	I/O	D	SCL	Serial clock input
50	F1	I	D	XCLR	System clear
51	F2	I	D	TEST2	TEST pin, 1.8V power supply
52	F3	GND	D	VSSLCB	1.2 V / 1.8 V GND
53	F4	Power	A	VDDHCM	2.9 V power supply
54	F8	Power	A	VDDHCM	2.9 V power supply
55	F9	GND	D	VSSLCB	1.2 V / 1.8 V GND
56	F10	I	D	XMASTER	Master / Slave selection Slave Mode: High Master Mode: Low
57	F11	I	D	SLAMODE1	Reference pin, Select slave address
58	G1	I	D	INCK	Master clock input
59	G2	GND	A	VSSLPLD	1.2 V / 1.8 V GND
60	G3	GND	A	VSSHPX	2.9 V GND
61	G4	Power	A	VDDHPX	2.9 V power supply
62	G8	Power	A	VDDHPX	2.9 V power supply
63	G9	GND	A	VSSHPX	2.9 V GND
64	G10	GND	A	VSSLPLD	1.2 V / 1.8 V GND
65	G11	Power	D	VDDMIO	1.8 V power supply
66	H1	GND	D	VSSLSC	1.2 V / 1.8 V GND
67	H2	GND	D	VSSLCN	1.2 V / 1.8 V GND
68	H3	GND	D	VSSLCB	1.2 V / 1.8 V GND
69	H4	Power	A	VDDHCM	2.9 V power supply
70	H8	Power	A	VDDHCM	2.9 V power supply
71	H9	GND	D	VSSLCB	1.2 V / 1.8 V GND
72	H10	GND	D	VSSLCN	1.2 V / 1.8 V GND
73	H11	GND	D	VSSLSC	1.2 V / 1.8 V GND
74	J1	Power	D	VDDLSC	1.2 V power supply
75	J2	Power	D	VDDLCN	1.2 V power supply
76	J3	GND	A	VSSLPL	1.2 V / 1.8 V GND
77	J4	GND	A	VSSLPLD	1.2 V / 1.8 V GND
78	J5	GND	A	VSSLPLA	1.2 V / 1.8 V GND
79	J6	—	—	N.C.	GND connectable
80	J7	—	—	N.C.	GND connectable
81	J8	—	—	N.C.	GND connectable
82	J9	—	—	N.C.	GND connectable
83	J10	Power	D	VDDLCN	1.2 V power supply
84	J11	Power	D	VDDLSC	1.2 V power supply
85	K1	O	D	DMO3N	CSI-2 output
86	K2	O	D	DMO3P	CSI-2 output
87	K3	Power	A	VDDLPL	1.2 V power supply
88	K4	Power	A	VDDLPLD	1.2 V power supply
89	K5	Power	A	VDDLPLA	1.2 V power supply
90	K6	—	—	N.C.	GND connectable
91	K7	—	—	N.C.	GND connectable
92	K8	—	—	N.C.	GND connectable
93	K9	—	—	N.C.	GND connectable

No.	Pin No	I/O	Analog / Digital	Symbol	Description
94	K10	O	D	DMO8P	CSI-2 output
95	K11	O	D	DMO8N	CSI-2 output
96	L1	O	D	DMO1N	CSI-2 output
97	L2	O	D	DMO1P	CSI-2 output
98	L3	GND	D	VSSLIF	1.2 V / 1.8 V GND
99	L4	GND	D	VSSLIF	1.2 V / 1.8 V GND
100	L5	GND	D	VSSLIF	1.2 V / 1.8 V GND
101	L6	Power	D	VDDLIF	1.2 V power supply
102	L7	GND	D	VSSLIF	1.2 V / 1.8 V GND
103	L8	GND	D	VSSLIF	1.2 V / 1.8 V GND
104	L9	GND	D	VSSLIF	1.2 V / 1.8 V GND
105	L10	O	D	DMO6P	CSI-2 output
106	L11	O	D	DMO6N	CSI-2 output
107	M3	O	D	DCK1P	CSI-2 clock output
108	M4	O	D	DMO2P	CSI-2 output
109	M5	O	D	DMO4P	CSI-2 output
110	M6	GND	D	VSSLSC	1.2 V / 1.8 V GND
111	M7	O	D	DMO7P	CSI-2 output
112	M8	O	D	DMO5P	CSI-2 output
113	M9	O	D	DCK2P	CSI-2 clock output
114	N1	—	—	N.C.	GND connectable
115	N3	O	D	DCK1N	CSI-2 clock output
116	N4	O	D	DMO2N	CSI-2 output
117	N5	O	D	DMO4N	CSI-2 output
118	N6	Power	D	VDDLSC	1.2 V power supply
119	N7	O	D	DMO7N	CSI-2 output
120	N8	O	D	DMO5N	CSI-2 output
121	N9	O	D	DCK2N	CSI-2 clock output
122	N11	—	—	N.C.	GND connectable

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDDHx VDDSUB	AV_{DD}		2.80	2.90	3.00	V
	Interface	VDDMx	OV_{DD}		1.70	1.80	1.90	V
	Digital	VDDLx	DV_{DD}		1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER SLAMODE0 SLAMODE1 SDA SCL TEST2	VIH	XVS / XHS Slave Mode	0.8 × OV_{DD}	—	—	V
			VIL		—	—	0.2 × OV_{DD}	V
Digital output voltage		XHS XVS TOUT TEST1	VOH	XVS / XHS Master Mode	OV_{DD} – 0.2	—	—	V
			VOL		—	—	0.2	V

Current Consumption

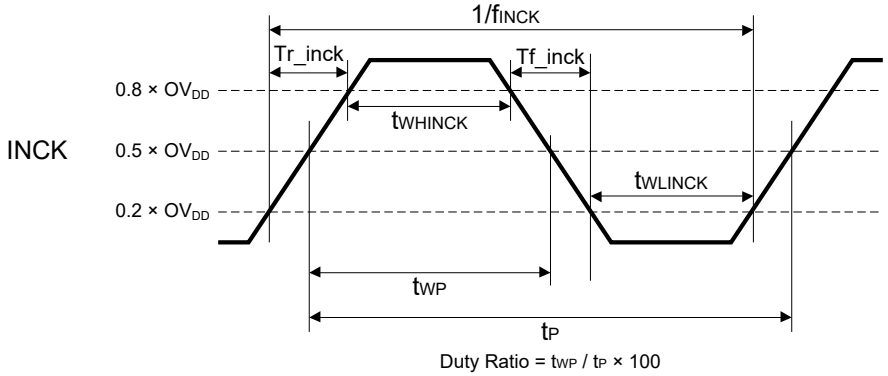
Item	Symbol	Typ.	Max.	Unit
Operating current MIPI CSI-2 / 4Lane × 2ch, 1188 Mbps 10 bit, 90.1 frame/s All-pixel mode	I_{AVDD}	127	197	mA
	I_{OVDD}	1	1	mA
	I_{DVDD}	347	587	mA
Standby current	I_{AVDD_STB}	—	0.1	mA
	I_{OVDD_STB}	—	0.1	mA
	I_{DVDD_STB}	—	50	mA

Operating current: (Typ.) Supply voltage 2.9 V / 1.8 V / 1.2 V, Tj = 25 ˚C, standard luminous intensity.
(Max.) Supply voltage 3.0 V / 1.9 V / 1.3 V, Tj = 60 ˚C, worst state of internal circuit operating current consumption,

Standby: (Max.) Supply voltage 3.0 V / 1.9 V / 1.3 V, Tj = 60 ˚C, INCK: 0 V, light-obstructed state.

AC Characteristics

Master Clock Waveform (INCK)



INCK 37.125MHz, 74.25MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	45	50	55	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %

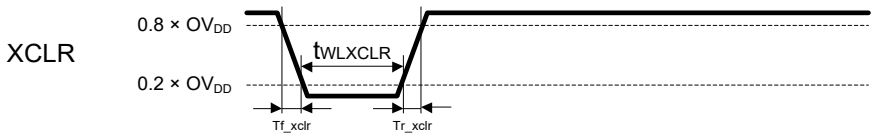
* The INCK fluctuation affects the frame rate.

INCK 6 to 27MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	6	—	27	MHz	f_{INCK} = 6 to 27MHz
INCK Low level pulse width	t_{WLINCK}	5	—	—	ns	
INCK High level pulse width	t_{WHINCK}	5	—	—	ns	
INCK clock duty	—	45	50	55	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %

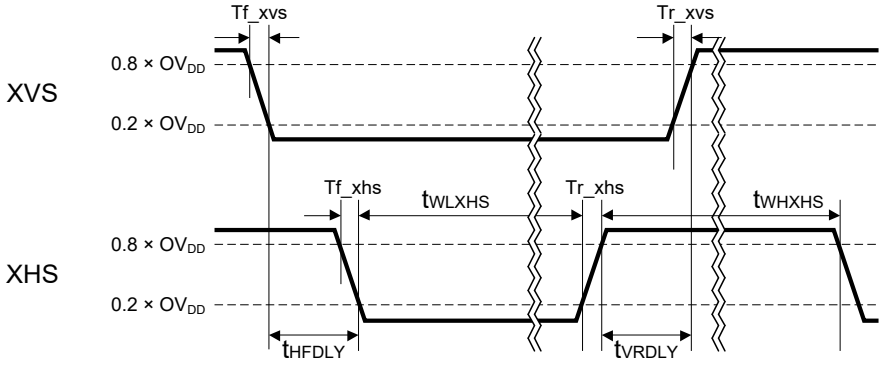
* The INCK fluctuation affects the frame rate.

System Clear (XCLR)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XCLR Low level pulse width	t_{WLXCLR}	100	—	—	ns	
XCLR Rise time	Tr_xclr	—	—	5	ns	20 % to 80 %
XCLR Fall time	Tf_xclr	—	—	5	ns	80 % to 20 %

XVS / XHS Input Characteristics in Slave Mode (XMASTER pin = High)



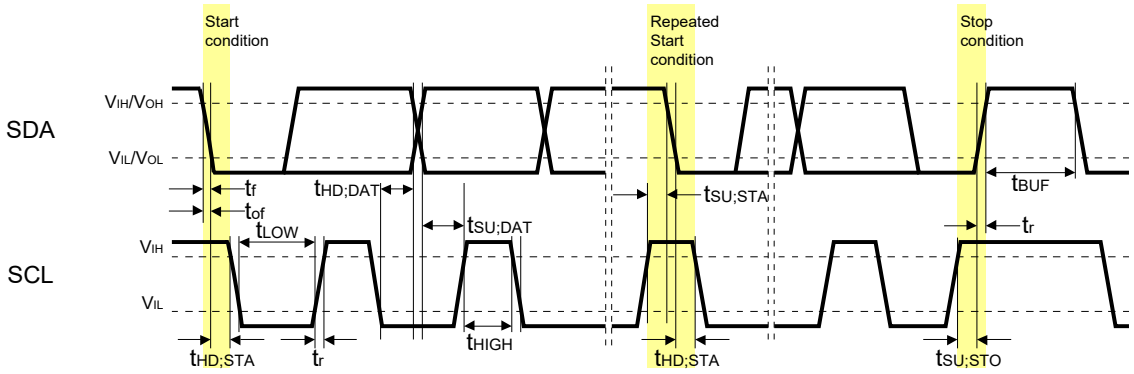
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	4 / f_{INCK}	—	—	ns	
XHS High level pulse width	t_{WHXHS}	4 / f_{INCK}	—	—	ns	
XVS - XHS fall width	t_{HFDLY}	0	—	—	ns	
XHS - XVS rise width	t_{VRDLY}	1 / f_{INCK}	—	—	ns	
XVS Rise time	Tr_xvs	—	—	5	ns	20 % to 80 %
XVS Fall time	Tf_xvs	—	—	5	ns	80 % to 20 %
XHS Rise time	Tr_xhs	—	—	5	ns	20 % to 80 %
XHS Fall time	Tf_xhs	—	—	5	ns	80 % to 20 %

XVS / XHS Input Characteristics in Master Mode (XMASTER pin = Low)

* XVS and XHS cannot be used for the sync signal to pixels.
  Be sure to detect sync code to detect the start of effective pixels in 1 line.
  For the output waveforms in master mode, see the item of “Slave Mode and Master Mode”

Serial Communication

I²C



I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	–0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OVDD < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Input current	Ii	–10	—	10	μA	0.1 × OV_{DD} – 0.9 × OV_{DD}
Input Capacitance for SCL / SDA	Ci	—	—	10	pF	

I²C AC Characteristics (Standard-mode, Fast-mode)

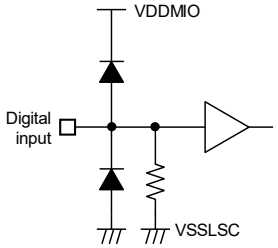
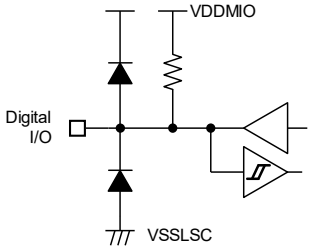
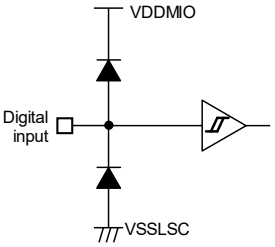
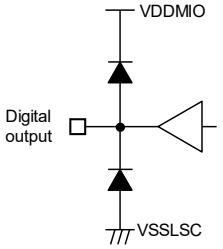
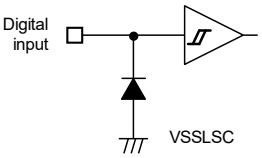
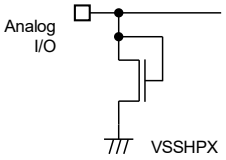
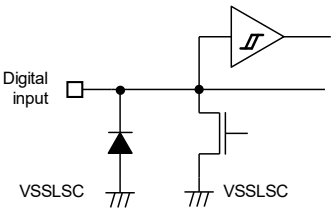
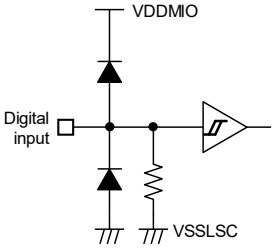
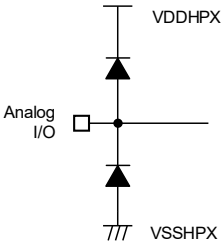
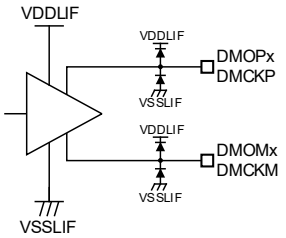
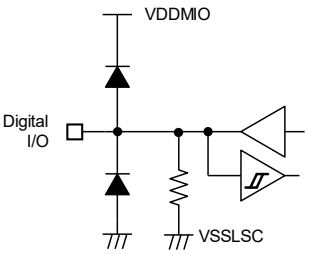
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCL clock frequency	f_{SCL}	0	—	400	kHz	
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	μs	
Low period of the SCL clock	t_{LOW}	1.3	—	—	μs	
High period of the SCL clock	t_{HIGH}	0.6	—	—	μs	
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	μs	
Data hold time	$t_{HD;DAT}$	0	—	0.9	μs	
Data set-up time	$t_{SU;DAT}$	100	—	—	ns	
Rise time of both SDA and SCL signals	t_r	—	—	300	ns	
Fall time of both SDA and SCL signals	t_f	—	—	300	ns	
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	μs	
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	μs	
Output fall time	tof	—	—	250	ns	Load 10 pF to 400 pF, 0.7 × OV_{DD} to 0.3 × OV_{DD}

I²C AC Characteristics (Fast-mode Plus)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCL clock frequency	f_{SCL}	0	—	1000	kHz	INCK ≥ 16 MHz
Hold time (Start Condition)	$t_{HD;STA}$	0.26	—	—	µs	
Low period of the SCL clock	t_{LOW}	0.5	—	—	µs	
High period of the SCL clock	t_{HIGH}	0.26	—	—	µs	
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.26	—	—	µs	
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs	
Data set-up time	$t_{SU;DAT}$	50	—	—	ns	
Rise time of both SDA and SCL signals	t_r	—	—	120	ns	
Fall time of both SDA and SCL signals	t_f	—	—	120	ns	
Set-up time (Stop Condition)	$t_{SU;STO}$	0.26	—	—	µs	
Bus free time between a STOP and START Condition	t_{BUF}	0.5	—	—	µs	
Output fall time	tof	—	—	120	ns	Load 10 pF to 400 pF, 0.7 × OV_{DD} to 0.3 × OV_{DD}

I/O Equivalent Circuit Diagram

□: External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
TENABLE		XVS XHS	
XMASTER TEST2		TEST1	
XCLR INCK		VRLFR VRLST	
SDA SCL		SLAMODE0 SLAMODE1	
VLOADLM1 VLOADLM2 VBGR ASMON1 ASMON2		DMOxP DMOxM DMCKxP DMCKxM	
TOUT			

Spectral Sensitivity Characteristics

(Characteristics in the wafer status)

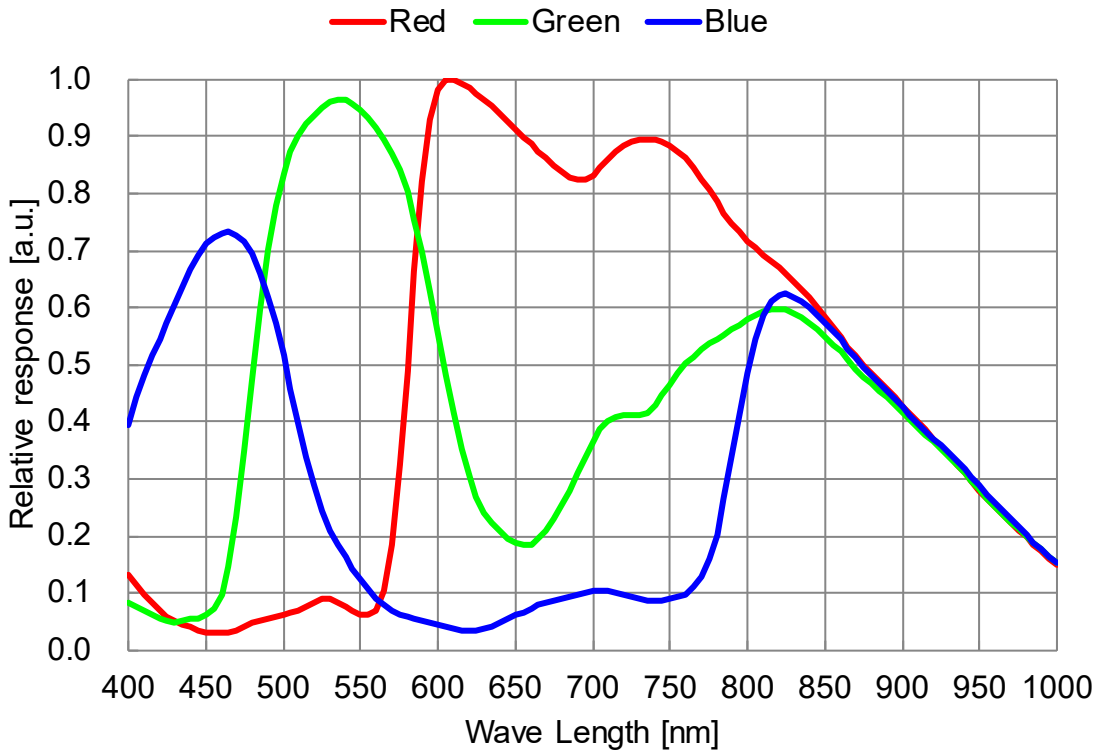


Image Sensor Characteristics

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, All-pixel mode, 12 bit 30 frame/s, Gain: 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		S	8104 (1860)	9530 (2188)	—	Digit (mV)	1	1/30 s storage 12 bit converted value HCG mode
			3093 (710)	3642 (836)	—	Digit (mV)		1/30 s storage 12 bit converted value LCG mode
Sensitivity ratio	R / G	RG	0.47	—	0.61	—	2	—
	B / G	BG	0.33	—	0.47	—		
Saturation signal		Vsat	3895 (894)	—	—	Digit (mV)	3	12 bit converted value LCG mode
Video signal shading		SH	—	—	25	%	4	—
Vertical line		VL	—	—	90	μV	5	12 bit converted value LCG mode
Dark signal		Vdt	—	—	0.66 (0.15)	Digit (mV)	6	1/30 s storage 12 bit converted value LCG mode
Dark signal shading		ΔVdt	—	—	0.66 (0.15)	Digit (mV)	7	1/30 s storage 12 bit converted value LCG mode
Conversion efficiency ratio		Rcg	2.3	2.6	2.8	—	8	HCG mode / LCG mode

Note) 1. Converted value into mV using 1Digit = 0.2295 mV for 12-bit output and 1Digit = 0.918 mV for 10-bit output.

2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the seal glass.

3. The characteristics above apply to effective pixel area.

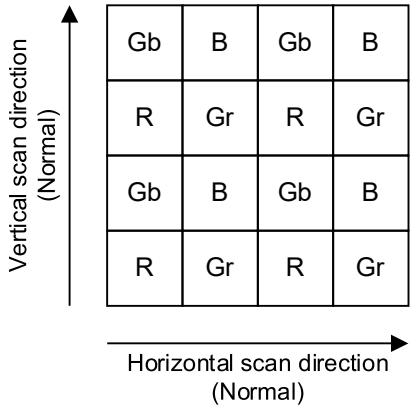
Image Sensor Characteristics Measurement Method

Measurement Conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.



Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   S = (VGr + VGb) / 2 × 100 / 30 [mV]

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to 836 mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   VG = (VGr + VGb) / 2
   RG = VR / VG
   BG = VB / VG

3. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 836 mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 836 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   SH = (Gmax – Gmin) / 836 × 100 [%]

5. Vertical Line
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, calculates each average output of Gr, Gb, R and B on respective columns. Calculates maximum value of difference with adjacent column on the same color (VL [μV]).

6. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

7. Dark signal shading
   After the measurement item 6, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

   ΔVdt = Vdmax – Vdmin [mV]

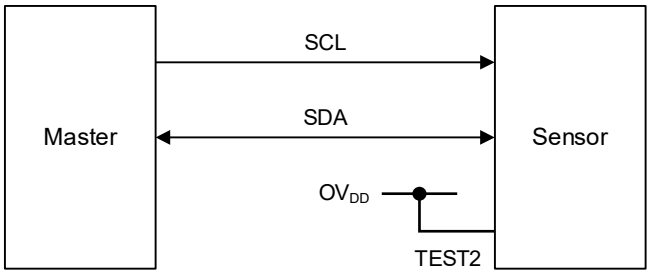
8. Conversion efficiency ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr And Gb and Gb signal outputs to 500 mV at the LCG mode, measure the average values of Gr and Gb signal output and calculate the ratio between HCG mode and LCG mode.

Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by I^2C communication. See the Register Map for the addresses and setting values to be set.

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions. Using SLAMODE0 and SLAMODE1 pins, SLAVE address can be changed.



Pin connection of serial communication

SLAVE Address

SLAMODE1 pin	SLAMODE0 pin	MSB							LSB
Low	Low	0	0	1	1	0	1	0	R / W
Low	High	0	0	1	0	0	0	0	R / W
High	Low	0	1	1	0	1	1	0	R / W
High	High	0	1	1	0	1	1	1	R / W

* R/W is data direction bit

R / W

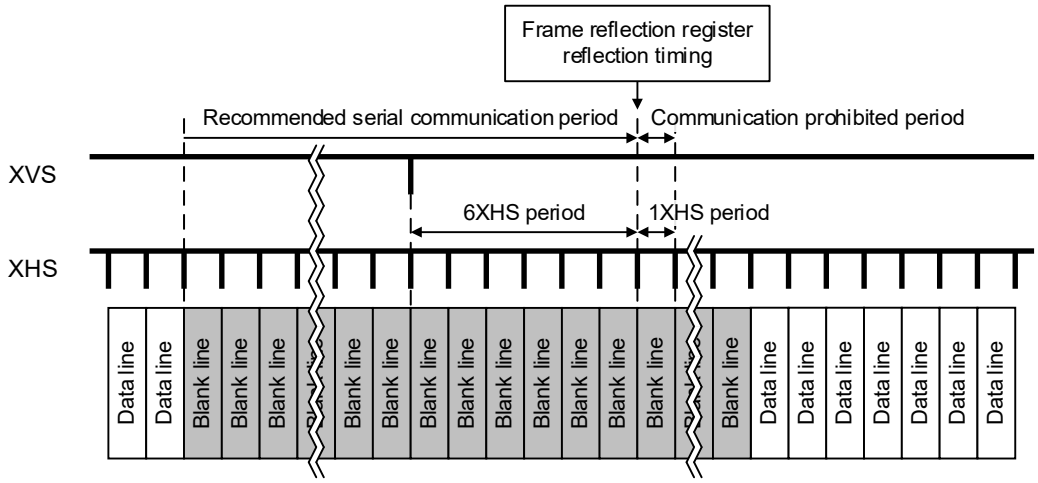
R / W bit	Data direction
0	Write (Master to Sensor)
1	Read (Sensor to Master)

I^2C pin description

Symbol	Pin No.	Remarks
SCL	E11	I^2C serial clock input
SDA	C10	I^2C serial data communication

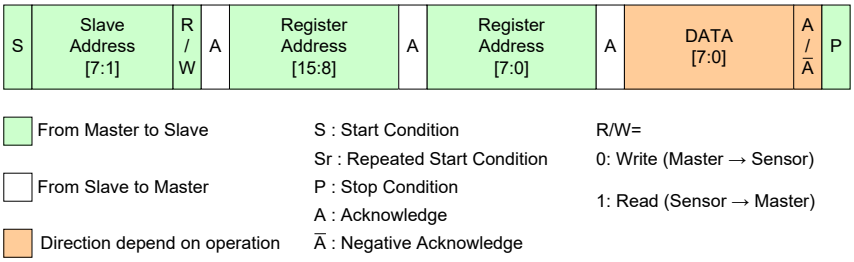
Register Communication Timing (I²C)

In I2C communication system, communication can be performed excluding the prohibited 1H period as described in the below figure.
For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by “Frame reflection register reflection timing”.
For the registers marked “I” in the item of Reflection timing, the settings are reflected when the communication is performed.
Using REGHOLD function is recommended for register setting using I²C communication. For REGHOLD function, see “Register Transmission Setting” in “Description of Functions”.



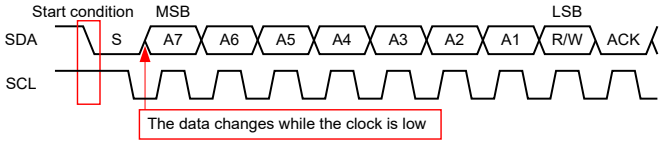
Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

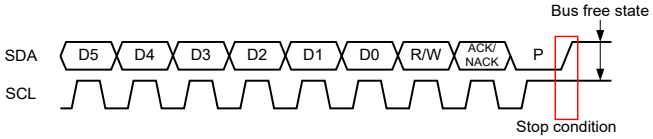


Communication Protocol

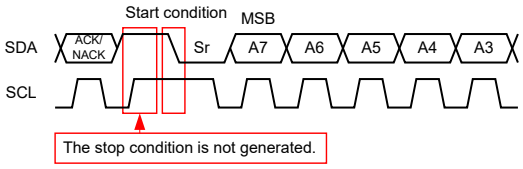
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / $\overline{A}$ (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SCL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

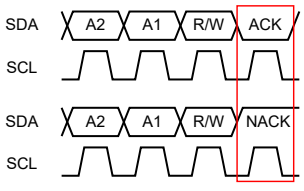


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



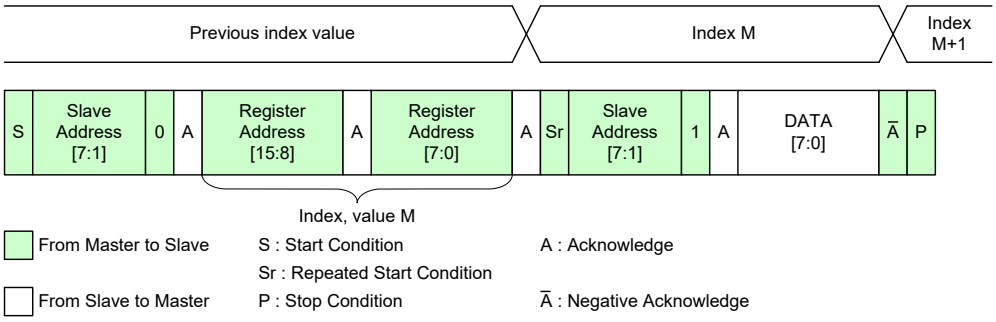
Acknowledge and Negative Acknowledge

Register Write and Read (I^2C)

This sensor corresponds to four reed modes and the two write modes.

Single Read from Random Location

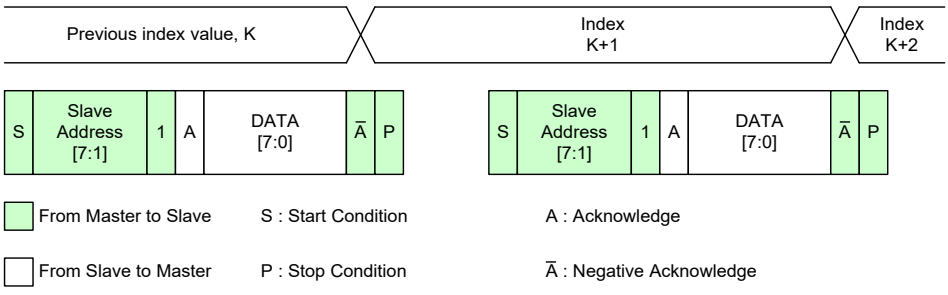
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose, it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication



Single Read from Random Location

Single Read from Current Location

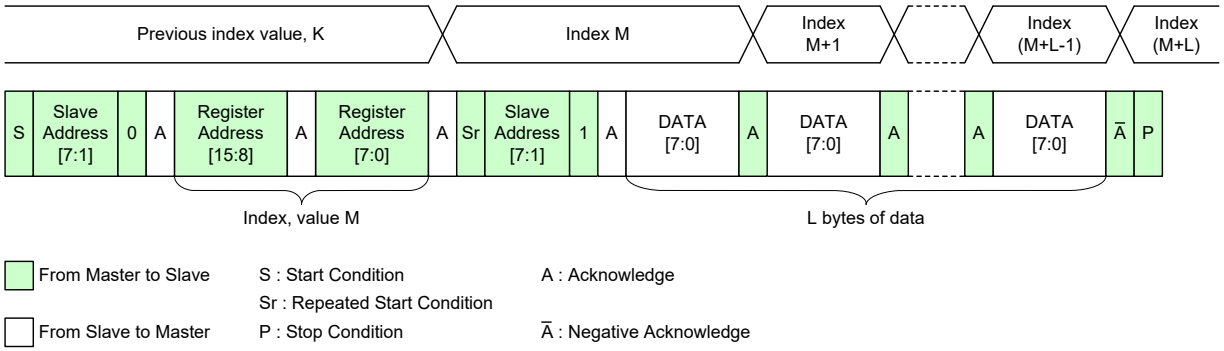
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

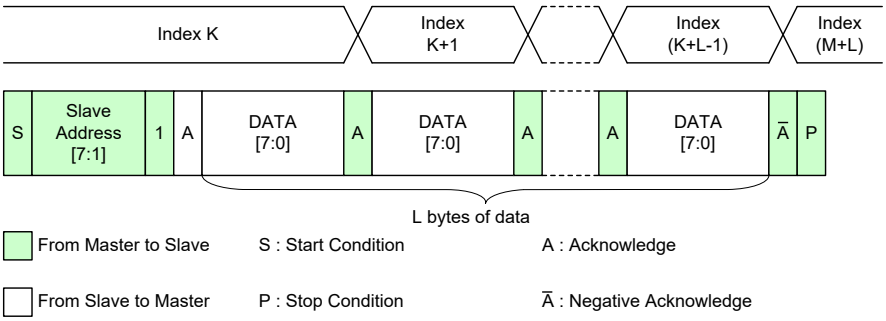
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition.
Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

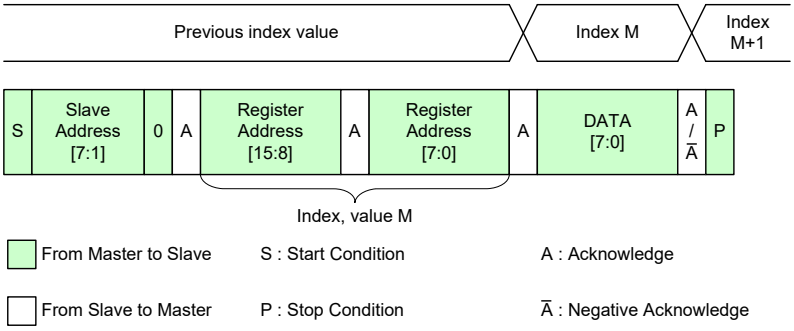
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA.
This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

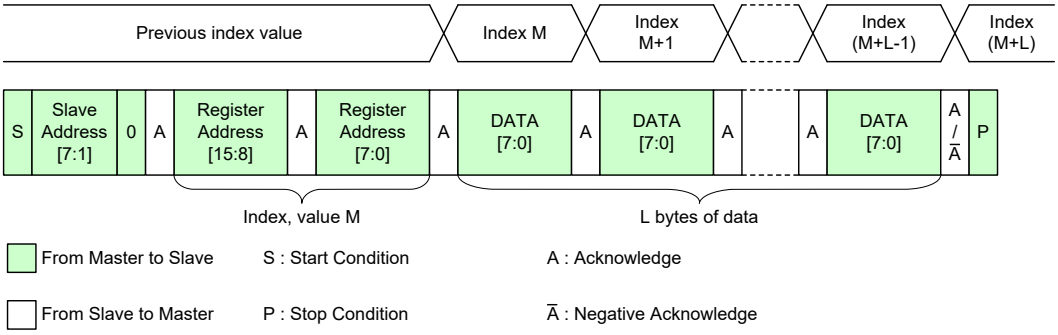
The Master sets the sensor index value to M by designating the sensor slave address with a write request and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

This sensor has a total of 3840 bytes (256 × 15) of registers, composed of registers with LSB addresses 00h to FFh that correspond to MSB address 30h to 3Eh. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 3840 bytes.

There are three different register reflection timings.
About the Reflection timing column of the Register Map, registers noted as "I" are reflected immediately after writing to register, registers noted as "S" are set during standby mode and reflected after standby canceled, registers noted as "V" are reflected at “Fame reflection register reflection timing” on the figure described in the section of “Setting Registers with Serial Communication”.

Do not perform communication to addresses not listed in the Register Map. Doing so may result in operation errors. However, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for LSB address; 3000h to 3EFFh.

* For the register that is writing " * " to the setting value in description (Indicated by red letter), change the value from the default value after the reset.
** In Gain setting only, it is reflected on the next frame which was settings.
*** Setting except for the setting values described in the description column is prohibited.

(1) Registers corresponding to address = 30**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3000h	0	STANDBY	Standby 0: Operating 1: Standby	1h	01h	I
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3001h	0	REGHOLD	Register hold (Function not to update V reflection register) 0: Invalid 1: Valid	0h	00h	I
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3002h	0	XMSTA	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1h	01h	I
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3008h	0	BCWAIT_TIME [9:0]	LSB	0FFh	FFh	S
	1					
	2					
	3					
	4		The value is set according to INCK. Refer to “INCK setting”			
	5					
	6					
	7					
3009h	0				00h	
	1		MSB			
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
300Ah	0	CPWAIT_TIME [9:0]	LSB	0B6h	B6h	S
	1					
	2					
	3					
	4		The value is set according to INCK. Refer to “INCK setting”			
	5					
	6					
	7					
300Bh	0				A0h	
	1		MSB			
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	EFWAIT_TIME [7:4]	The value is set according to INCK. Refer to “INCK setting”	Ah		S
	5					
	6					
	7					
301Ch	0	WINMODE [3:0]	Window mode setting 0: All-pixel mode 4: Window cropping mode	0h	00h	V
	1					
	2					
	3					
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3020h	0	HADD	Mode setting 0h: All-pixel mode 1h: Horizontal 2 binning	0h	00h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3021h	0	VADD	Mode setting 0h: All-pixel mode 1h: Vertical 2 binning	0h	00h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3022h	0	ADDMODE [1:0]	Mode setting 0h: Non-binning 1h: Horizontal/Vertical 2/2-line binning	0h	00h	S
	1					
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3024h	0	VMAX [19:0]	LSB	008CAh	CAh	V
	1					
	2					
	3					
	4					
	5					
	6		When sensor master mode vertical span setting.			
	7					
3025h	0		For details, see the item of “Slave Mode and Master Mode” in the section of “Description of Various Functions”.		08h	
	1					
	2					
	3					
	4					
	5		Multiples of 2			
	6					
	7					
3026h	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3028h	0	HMAX [15:0]	LSB	0226h	26h	V
	1					
	2					
	3					
	4					
	5		When sensor master mode horizontal span setting.			
	6					
	7					
3029h	0		For details, see the item of “Slave Mode and Master Mode” in the section of “Description of Various Functions”.		02h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3030h	0	HREVERSE	Horizontal direction Readout inversion control 0: Normal 1: Inverted	0h	00h	V
	1	VREVERSE	Vertical direction Readout inversion control 0: Normal 1: Inverted	0h		V
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3031h	0	ADBIT	AD conversion bits setting 0: AD 10 bit 1: AD 12 bit	1h	01h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3032h	0	MDBIT	Number of output bit setting 0: 10 bit 1: 12 bit	1h	01h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3034h	0	FDG_SEL0	Conversion gain switching 0: LCG Mode 1: HCG Mode	0h	00h	V
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
303Ch	0	PIX_HST [12:0]	LSB In window cropping mode Start position (Horizontal direction) Multiples of 2 (Non-binning) Multiples of 4 (Horizontal/Vertical 2/2-line binning)	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
303Dh	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
303Eh	0	PIX_HWIDTH [12:0]	LSB In window cropping mode Cropping width (Horizontal direction) Multiples of 12 (Non-binning) Multiples of 24 (Horizontal/Vertical 2/2-line binning)	0F18h	18h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
303Fh	0				0Fh	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3040h	0	XSIZE_OVERLAP [10:0]	LSB In MIPI 4Lane × 2ch The number of right and left division H direction overlap pixels(MAX 1008d(3F0h)) Multiples of 12 Smaller than PIX_HWIDTH	000h	00h	S
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3041h	0				00h	
	1					
	2		MSB			
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3044h	0	PIX_VST [11:0]	LSB In window cropping mode Start position (Vertical direction) Multiples of 2 (Non-binning) Multiples of 4 (Horizontal/Vertical 2/2-line binning)	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3045h	0				00h	
	1					
	2		MSB			
	3					
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3046h	0	PIX_VWIDTH [11:0]	LSB In window cropping mode Start position (Vertical direction) Multiples of 2 (Non-binning) Multiples of 4 (Horizontal/Vertical 2/2-line binning)	884h	84h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3047h	0				08h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3050h	0	SHR0 [19:0]	LSB	00066h	66h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3051h	0		Storage time adjustment Designated in line units. Multiples of 2		00h	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3052h	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3084h	0	GAIN [10:0]	LSB	000h	00h	V
	1					
	2					
	3					
	4					
	5		Gain setting (0.0dB to 72dB / 0.3dB step)			
	6					
	7					
3085h	0				00h	
	1					
	2		MSB			
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30A4h	0	XVSOUTSEL [1:0]	XVS pin setting in master mode 0: Fixed to Low 2: VSYNC output	2h	2Ah	I
	1					
	2	XHSOUTSEL [1:0]	XHS pin setting in master mode 0: Fixed to Low 2: HSYNC output	2h		I
	3					
	4	—	Fixed to “2h”	2h		—
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
30A5h	0	XVS_DRV [1:0]	XVS pin setting 0: XVS output (Master mode) 3: HiZ (Slave mode)	3h	0Fh	S
	1					
	2	XHS_DRV [1:0]	XHS pin setting 0: XHS output (Master mode) 3: HiZ (Slave mode)	3h		S
	3					
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30CCh	0	—	Fixed to “0h”	0h	00h	—
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	XVSLNG [1:0]	XVS pulse width setting in master mode. 0: 1H 1: 2H 2: 4H 3: 8H	0h		I
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30CDh	0	—	Fixed to “0h”	0h	00h	—
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	XHSLNG [1:0]	XHS pulse width setting in master mode. 0: 16clock 1: 32clock 2: 64clock 3: 128clock	0h		I
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30D5h	0	DIG_CLP_VSTART	The value is set according to Readout mode. 2: Horizontal / Vertical 2/2-line binning mode 4: All-pixel scan mode	04h	04h	V
	1					
	2					
	3					
	4					
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
30DCh	0	BLKLEVEL [9:0]	LSB	032h	32h	S
	1					
	2					
	3		Black level offset value setting			
	4					
	5		10-bit readout mode: 1digit/1h			
	6		12-bit readout mode: 4digit/1h			
	7					
30DDh	0				00h	
	1		MSB			
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

(2) Registers corresponding to address = 31**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3114h	0	INCKSEL1 [1:0]	The value is set according to INCK. Refer to “INCK setting”	03h	03h	S
	1					
	2	—	Fixed to “0h”			
	3	—	Fixed to “0h”			
	4	—	Fixed to “0h”			
	5	—	Fixed to “0h”			
	6	—	Fixed to “0h”			
	7	—	Fixed to “0h”			
3119h	0	INCKSEL2 [1:0]	The value is set according to INCK. Refer to “INCK setting”	00h	00h	S
	1					
	2	—	Fixed to “0h”			
	3	—	Fixed to “0h”			
	4	—	Fixed to “0h”			
	5	—	Fixed to “0h”			
	6	—	Fixed to “0h”			
	7	—	Fixed to “0h”			

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
311Ch	0	INCKSEL3 [8:0]	The value is set according to INCK. Refer to “INCK setting”	0C0h	C0h	S
	1					
	2					
	3					
	4					
	5					
	6					
	7					
311Dh	0				00h	
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

(3) Registers corresponding to address = 32**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3260h	[7:0]	—	Set to “22h”	20h	20h	S
3262h	[7:0]	—	Set to “02h”	03h	03h	S
3278h	[7:0]	—	Set to “A2h”	A0h	A0h	S

(4) Registers corresponding to address = 33**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3324h	[7:0]	—	Set to “00h”	01h	01h	S
3366h	[7:0]	—	Set to “31h”	0Dh	0Dh	S

(5) Registers corresponding to address = 34**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By Address	
340Ch	[7:0]	—	Set to “4Dh”	4Ah	4Ah	S
3416h	[7:0]	—	Set to “10h”	06h	06h	S
3417h	[7:0]	—	Set to “13h”	09h	09h	S
3432h	[7:0]	—	Set to “93h”	FEh	FEh	S
34CEh	[7:0]	—	Set to “1Eh”	00h	00h	S
34CFh	[7:0]	—	Set to “1Eh”	00h	00h	S
34DCh	[7:0]	—	Set to “80h”	4Ah	4Ah	S

(6) Registers corresponding to address = 35**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
351Ch	[7:0]	—	Set to “03h”	02h	02h	S
359Eh	[7:0]	—	Set to “70h”	8Fh	8Fh	S
35A2h	[7:0]	—	Set to “9Ch”	EDh	EDh	S
35ACh	[7:0]	—	Set to “08h”	00h	00h	S
35C0h	[7:0]	—	Set to “FAh”	FCh	FCh	S
35C2h	[7:0]	—	Set to “4Eh”	32h	32h	S

(7) Registers corresponding to address = 36**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3608h	[7:0]	—	Set to “41h”	3Eh	3Eh	S
360Ah	[7:0]	—	Set to “47h”	44h	44h	S
361Eh	[7:0]	—	Set to “4Ah”	47h	47h	S
3630h	[7:0]	—	Set to “43h”	40h	40h	S
3632h	[7:0]	—	Set to “47h”	44h	44h	S
363Ch	[7:0]	—	Set to “41h”	3Eh	3Eh	S
363Eh	[7:0]	—	Set to “4Ah”	47h	47h	S
3648h	[7:0]	—	Set to “41h”	3Eh	3Eh	S
364Ah	[7:0]	—	Set to “47h”	44h	44h	S
3660h	[7:0]	—	Set to “04h”	00h	00h	S
3676h	[7:0]	—	Set to “3Fh”	3Ch	3Ch	S
367Ah	[7:0]	—	Set to “3Fh”	3Ch	3Ch	S
36A4h	[7:0]	—	Set to “41h”	3Eh	3Eh	S

(8) Registers corresponding to address = 37**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3798h	[7:0]	—	Set to “82h”	69h	69h	S
379Ah	[7:0]	—	Set to “82h”	69h	69h	S
379Ch	[7:0]	—	Set to “82h”	69h	69h	S
379Eh	[7:0]	—	Set to “82h”	69h	69h	S

(9) Registers corresponding to address = 38**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3804h	0	INCKSEL4 [1:0]	The value is set according to INCK. Refer to “INCK setting”	23h	23h	S
	1					
	2	—	Set to “0h”			
	3	—	Set to “0h”			
	4	—	Set to “0h”			
	5	—	Set to “1h”			
	6	—	Set to “0h”			
	7	—	Set to “0h”			
3807h	0	INCKSEL5 [7:0]	The value is set according to INCK. Refer to “INCK setting”	60h	60h	S
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3888h	[7:0]	—	Set to “A8h”	9Ch	9Ch	S
388Ch	[7:0]	—	Set to “A6h”	9Ah	9Ah	S

(10)Registers corresponding to address = 39**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3914h	[7:0]	—	Set to “15h”	1Bh	1Bh	S
3915h	[7:0]	—	Set to “15h”	1Bh	1Bh	S
3916h	[7:0]	—	Set to “15h”	1Ah	1Ah	S
3917h	[7:0]	—	Set to “14h”	19h	19h	S
3918h	[7:0]	—	Set to “14h”	17h	17h	S
3919h	[7:0]	—	Set to “14h”	0Fh	0Fh	S
391Ah	[7:0]	—	Set to “13h”	0Bh	0Bh	S
391Bh	[7:0]	—	Set to “13h”	0Bh	0Bh	S
391Ch	[7:0]	—	Set to “13h”	0Bh	0Bh	S
391Eh	[7:0]	—	Set to “00h”	11h	11h	S
391Fh	[7:0]	—	Set to “A5h”	43h	43h	S
3920h	[7:0]	—	Set to “DEh”	76h	76h	S
3921h	[7:0]	—	Set to “0Eh”	07h	07h	S
39A2h	[7:0]	—	Set to “0Ch”	2Bh	2Bh	S
39A4h	[7:0]	—	Set to “16h”	FFh	FFh	S
39A6h	[7:0]	—	Set to “2Bh”	00h	00h	S
39A7h	[7:0]	—	Set to “01h”	00h	00h	S
39D2h	[7:0]	—	Set to “2Dh”	9Bh	9Bh	S
39D3h	[7:0]	—	Set to “00h”	01h	01h	S
39D8h	[7:0]	—	Set to “37h”	FFh	FFh	S
39D9h	[7:0]	—	Set to “00h”	01h	01h	S
39DAh	[7:0]	—	Set to “9Bh”	00h	00h	S
39DBh	[7:0]	—	Set to “01h”	00h	00h	S
39E0h	[7:0]	—	Set to “28h”	96h	96h	S
39E1h	[7:0]	—	Set to “00h”	01h	01h	S
39E2h	[7:0]	—	Set to “2Ch”	9Ah	9Ah	S
39E3h	[7:0]	—	Set to “00h”	01h	01h	S
39E8h	[7:0]	—	Set to “96h”	FFh	FFh	S

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
39EAh	[7:0]	—	Set to “9Ah”	00h	00h	S
39EBh	[7:0]	—	Set to “01h”	00h	00h	S
39F2h	[7:0]	—	Set to “27h”	95h	95h	S
39F3h	[7:0]	—	Set to “00h”	01h	01h	S

(11)Registers corresponding to address = 3A**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3A00h	[7:0]	—	Set to “38h”	FFh	FFh	S
3A01h	[7:0]	—	Set to “00h”	01h	01h	S
3A02h	[7:0]	—	Set to “95h”	00h	00h	S
3A03h	[7:0]	—	Set to “01h”	00h	00h	S
3A18h	[7:0]	—	Set to “9Bh”	39h	39h	S
3A2Ah	[7:0]	—	Set to “0Ch”	31h	31h	S
3A30h	[7:0]	—	Set to “15h”	FFh	FFh	S
3A32h	[7:0]	—	Set to “31h”	00h	00h	S
3A33h	[7:0]	—	Set to “01h”	00h	00h	S
3A36h	[7:0]	—	Set to “4Dh”	38h	38h	S
3A3Eh	[7:0]	—	Set to “11h”	37h	37h	S
3A40h	[7:0]	—	Set to “31h”	FFh	FFh	S
3A42h	[7:0]	—	Set to “4Ch”	00h	00h	S
3A43h	[7:0]	—	Set to “01h”	00h	00h	S
3A44h	[7:0]	—	Set to “47h”	32h	32h	S
3A46h	[7:0]	—	Set to “4Bh”	36h	36h	S
3A4Eh	[7:0]	—	Set to “11h”	31h	31h	S
3A50h	[7:0]	—	Set to “32h”	FFh	FFh	S
3A52h	[7:0]	—	Set to “46h”	00h	00h	S
3A53h	[7:0]	—	Set to “01h”	00h	00h	S

(12)Registers corresponding to address = 3D**h.

Address	bit	Register name	Description	Default value		Reflection timing
				By register	By address	
3D01h	0 1 2	LANEMODE [2:0]	Output interface selection 1: CSI-2 2lane 3: CSI-2 4lane 6: CSI-2 4lane × 2ch 7: CSI-2 8lane	3h	03h	S
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3D04h	[7:0]	TXCLKESC_FREQ [15:0]	The value is set according to INCK. Refer to “INCK setting”	1290h	90h	S
3D05h	[7:0]				12h	
3D0Ch	0	INCKSEL6	The value is set according to INCK. Refer to “INCK setting”	1h	01h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3D18h	[7:0]	TCLKPOST [15:0]	The value is set according to Data Rate Refer to “Global Timing setting”	00B7h	B7h	S
3D19h	[7:0]				00h	
3D1Ah	[7:0]	TCLKPREPARE [15:0]	The value is set according to Data Rate Refer to “Global Timing setting”	0067h	67h	S
3D1Bh	[7:0]				00h	
3D1Ch	[7:0]	TCLKTRAIL [15:0]	The value is set according to Data Rate Refer to “Global Timing setting”	006Fh	6Fh	S
3D1Dh	[7:0]				00h	
3D1Eh	[7:0]	TCLKZERO [15:0]	The value is set according to Data Rate Refer to “Global Timing setting”	01DFh	DFh	S
3D1Fh	[7:0]				01h	
3D20h	[7:0]	THSPREPARE [15:0]	The value is set according to Data Rate Refer to “Global Timing setting”	006Fh	6Fh	S
3D21h	[7:0]				00h	
3D22h	[7:0]	THSZERO [15:0]	The value is set according to Data Rate Refer to “Global Timing setting”	00CFh	CFh	S
3D23h	[7:0]				00h	
3D24h	[7:0]	THSTRAIL [15:0]	The value is set according to Data Rate Refer to “Global Timing setting”	006Fh	6Fh	S
3D25h	[7:0]				00h	
3D26h	[7:0]	THSEXIT [15:0]	The value is set according to Data Rate Refer to “Global Timing setting”	00B7h	B7h	S
3D27h	[7:0]				00h	
3D28h	[7:0]	TLPX [15:0]	The value is set according to Data Rate Refer to “Global Timing setting”	005Fh	5Fh	S
3D29h	[7:0]				00h	

Readout Drive mode

Operating mode

The table below shows the operating modes available with this sensor.
These frame rates indicate the maximum rates for each mode. When using a typical frame rate, please refer to the "List of Setting Register" at section "Image Data Output Format".

Mode	Lane	Data rate [Mbps/Lane]	AD conversion [bit]	Output bit width [bit]	Frame rate [frame/s]	Recording Pixels H [pixels]	Recording Pixels V [lines]	INCK [MHz]	1H period [Clock]	1V period [XHS]
All pixel	2	1782	12	12	32.4	3840	2160	6-27, 37.125, 74.25	1018 (*1)	2250
			10	10	38.5				857 (*1)	
	4		12	12	60.0				550 (*1)	
			10	10	72.6				454 (*1)	
	8	891	12	12	60.0				550 (*1)	
		1188	10	10	90.1				366 (*1)	
	4×2ch	891	12	12	60.0				550 (*1)	
		1188	10	10	90.1				366 (*1)	
Horizontal/ Vertical 2/2-line binning	2	1782	10	12	61.6	1920	1080	6-27, 37.125, 74.25	535 (*1)	2250
	4	1440	10	12	90.1				366 (*1)	
	8	720	10	12	90.1				366 (*1)	
	4×2ch		10	12	90.1				366 (*1)	

(*1) Clock frequency = 74.25 [MHz]

Variable Data Rate

The table below shows the changing in the range available with "Data Rate".
About the setting , please refer to "INCK setting" and "Global timing setting".

Lane	Data Rate [Mbps / Lane]
2 Lane	594 to 891, 1188 to 1782
4 Lane	594 to 891, 1188 to 1782
8 Lane	594 to 891, 1188 to 1440
4 × 2 Lane	594 to 891, 1188 to 1440

Image Data Output Format (CSI-2 output)

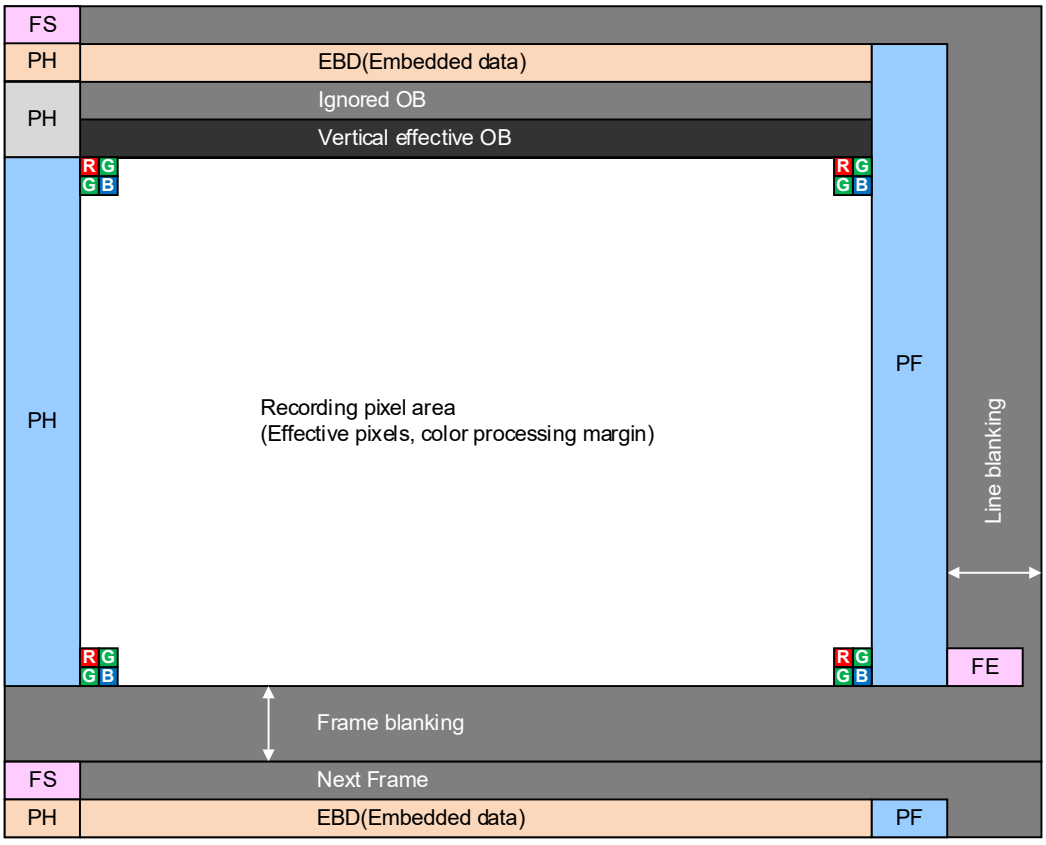
Frame Format

Each line of each image frame is output like the General Frame Format of CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Setting register (I^2C)	Description
00h	Frame Start Code	N/A	FS
01h	Frame End Code	N/A	FE
10h	NULL	N/A	Invalid data
12h	Embedded Data	N/A	Embedded data
2Bh	RAW10	Address: 3032h MDBIT [0]	0A0Ah
2Ch	RAW12		0C0Ch
37h	OB Data	N/A	Vertical OB line data

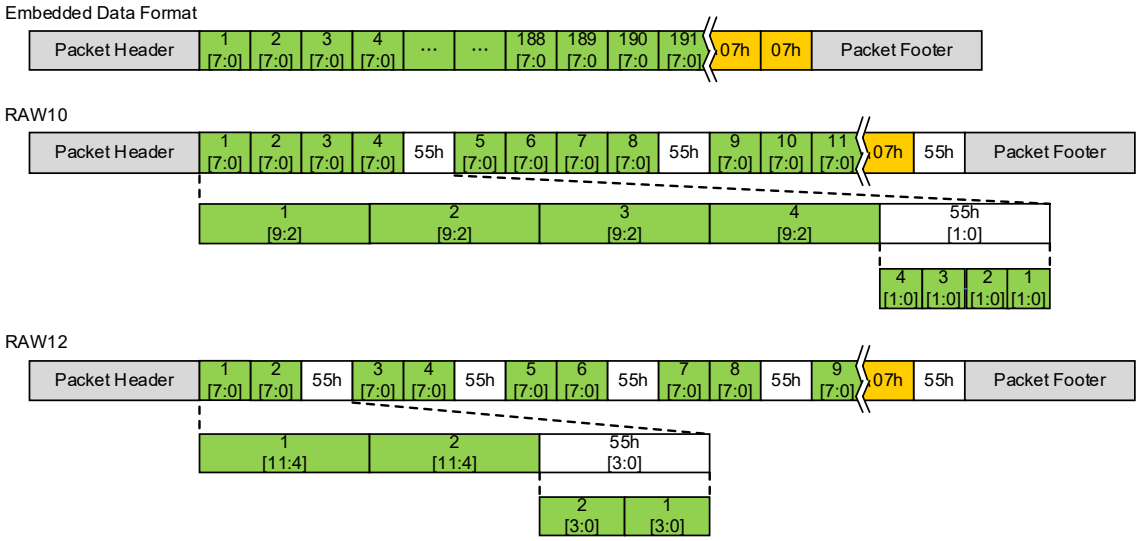
Frame Structure



Frame Structure of CSI-2 output

Embedded Data Line

The Embedded data line is output in a line following the sync code FS.



The end of the address and the register value is determined according to the tags embedded in the data.

Embedded Data Line Tag

Tag	Data Byte Description
00h	Illegal Tag. If found treat as end of Data.
07h	End of Data.
AAh	CCI Register Index MSB [15:8]
A5h	CCI Register Index LSB [7:0]
5Ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data.
55h	Auto increment the CCI index after the data byte – null data A CCI register does not exist for the current CCI index. The data byte value is the 07h.
FFh	Illegal Tag. If found treat as end of Data.

Specific output examples are shown below.

Pixel (8bit)	bit	I²C address [HEX]	Data Byte Description	Description
1	[7:0]	—	—	ignored
2	[3:0]	301C[3:0]	WINMODE	
3	[3:0]	—	—	ignored
	[4]	3030[0]	HREVERSE	
	[6:5]	3022[1:0]	ADDMODE	
	[7]	—	—	ignored
4 to 8	[7:0]	—	—	ignored
9	[4:0]	—	—	ignored
	[5]	3030[1]	VREVERSE	
	[7:6]	—	—	ignored
10	[7:0]	—	—	ignored
11	[5:0]	—	—	ignored
	[7]	3031[0]	ADBIT	
12	[7:0]	—	—	ignored
13	[2:0]	3D01[2:0]	LANEMODE	
	[3]	3032[0]	MDBIT	
	[7:4]	—	—	
18 to 23	[7:0]	—	—	ignored
24	[7:0]	3050[7:0]	SHR0	
25	[7:0]	3051[7:0]		
26	[3:0]	3052[3:0]		
	[7:4]	—	—	ignored
27 to 53	[7:0]	—	—	ignored
54	[7:0]	30DC[7:0]	BLKLEVEL	
55	[1:0]	30DD[1:0]		
	[7:2]	—	—	ignored
56 to 216	[7:0]	—	—	ignored

Output data is Data[7:0] = 00h from 217 to 224 pixel.
Output data is Data[7:0] = 07h from 225 to end pixel.

Image Data Output Format

The table below shows the register setting example of typical frame rate.
The frame rate is obtained by the following formula when using other frame rates.

Frame rate [frame / s] = 1 / (V_{TTL} × (1H period))

V_{TTL}	:	1 frame line length or VMAX
	:	“1V period” or more in “Operating mode”
1H period (unit [s])	:	“1H period” or more in “Operating mode”

All-pixel mode

List of Setting Register

Address	bit	Register Name	Initial Value	CSI-2 serial / 2lane		Remark
				30		[frame/s]
				1440	1782	[Mbps/lane]
				14.8	14.8	1Hperiod[μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	Refer to “INCK setting”		
3009h	[1:0]					
300Ah	[7:0]	CPWAIT_TIME	0B6h			
300Bh	[1:0]					
	[7:4]	EFWAIT_TIME	Ah			
301Ch	[3:0]	WINMODE	0h	0h		All pixel mode
3022h	[1:0]	ADDMODE	0h	0h		All pixel mode
3024h	[7:0]	VMAX	8CAh	8CAh		
3025h	[7:0]					
3026h	[3:0]					
3028h	[7:0]	HMAX	226h	44Ch		
3029h	[7:0]					
3030h	[0]	HREVERSE	0h	0h / 1h		0: Nor, 1: Inv
	[1]	VREVERSE	0h	0h / 1h		0: Nor, 1: Inv
3031h	[1:0]	ADBIT	1h	0h		0: 10 bit, 1: 12 bit
3032h	[0]	MDBIT	1h	0h		0: 10 bit, 1: 12 bit
3114h	[1:0]	INCKSEL1	3h	Refer to “INCK setting”		
3119h	[1:0]	INCKSEL2	0h			
311Ch	[7:0]	INCKSEL3	0C0h			
311Dh	[0]					
3152h to 37FFh	[7:0]	Refer to “Register Map”				
3804h	[1:0]	INCKSEL4	3h	Refer to “INCK setting”		
3807h	[7:0]	INCKSEL5	60h			
3888h to 3AFFh	[7:0]	Refer to “Register Map”				

Address	bit	Register Name	Initial Value	CSI-2 serial / 2lane		Remark
				30		[frame/s]
				1440	1782	[Mbps/lane]
3D01h	[2:0]	LANEMODE	3h	1h		2Lane
3D04h	[7:0]	TXCLCKES_FREQ	1290h	Refer to “INCK setting”		
3D05h	[7:0]					
3D0Ch	[0]	INCKSEL6	1h			
3D18h	[7:0]	TCLKPOST	00B7h	009Fh	00B7h	Global timing
3D19h	[7:0]					
3D1Ah	[7:0]	TCLKPREPARE	0067h	0057h	0067h	Global timing
3D1Bh	[7:0]					
3D1Ch	[7:0]	TCLKTRAIL	006Fh	0057h	006Fh	Global timing
3D1Dh	[7:0]					
3D1Eh	[7:0]	TCLKZERO	01DFh	0187h	01DFh	Global timing
3D1Fh	[7:0]					
3D20h	[7:0]	THSPREPARE	006Fh	005Fh	006Fh	Global timing
3D21h	[7:0]					
3D22h	[7:0]	THSZERO	00CFh	00A7h	00CFh	Global timing
3D23h	[7:0]					
3D24h	[7:0]	THSTRAIL	006Fh	005Fh	006Fh	Global timing
3D25h	[7:0]					
3D26h	[7:0]	THSEXIT	00B7h	0097h	00B7h	Global timing
3D27h	[7:0]					
3D28h	[7:0]	TLPX	005Fh	004Fh	005Fh	Global timing
3D29h	[7:0]					

Address	bit	Register Name	Initial Value	CSI-2 serial / 4lane					Remark
				15	30	60	30	60	[frame/s]
				594	720	1440		1782	[Mbps/lane]
				29.6	14.8	7.4	14.8	7.8	1H period[μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	Refer to “INCK setting”					
3009h	[1:0]								
300Ah	[7:0]	CPWAIT_TIME	0B6h						
300Bh	[1:0]								
	[7:4]	EFWAIT_TIME	Ah						
301Ch	[3:0]	WINMODE	0h	0h					All pixel mode
3022h	[1:0]	ADDMODE	0h	0h					All pixel mode
3024h	[7:0]	VMAX	8CAh	8CAh					
3025h	[7:0]								
3026h	[3:0]								
3028h	[7:0]	HMAX	226h	898h		44Ch	226h / 44Ch	226h	
3029h	[7:0]								
3030h	[0]	HREVERSE	0h	0h / 1h					0: Nor, 1: Inv
	[1]	VREVERSE	0h	0h / 1h					0: Nor, 1: Inv
3031h	[1:0]	ADBIT	1h	0h	1h	0h	0h	1h	1h	0: 10 bit, 1: 12 bit
3032h	[0]	MDBIT	1h	0h	1h	0h	0h	1h	1h	0: 10 bit, 1: 12 bit
3114h	[7:0]	INCKSEL1	00h	Refer to “INCK setting”					
3119h	[7:0]	INCKSEL2	28h						
311Ch	[7:0]	INCKSEL3	0C0h						
311Dh	[0]								
3152h to 37FFh	[7:0]	Refer to “Register Map”							
3804h	[1:0]	INCKSEL4	3h	Refer to “INCK setting”					
3807h	[7:0]	INCKSEL5	60h						
3888h to 3AFFh	[7:0]	Refer to “Register Map”							

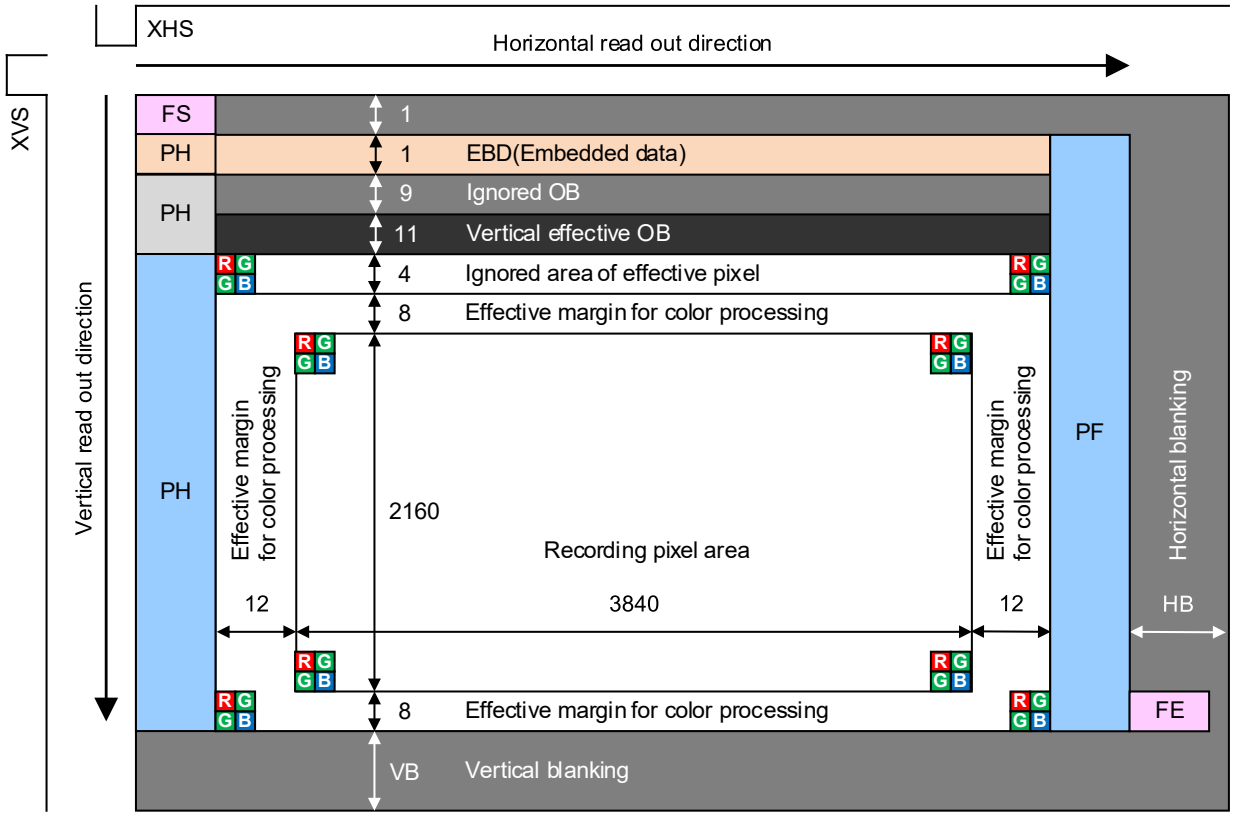
Address	bit	Register Name	Initial Value	CSI-2 serial / 4lane						Remark
				15		30	60	30	60	[frame/s]
				594		720	1440		1782	[Mbps/lane]
3D01h	[2:0]	LANEMODE	3h	3h						4lane
3D04h	[7:0]	TXCLCKES_FREQ	1290h	Refer to “INCK setting”						
3D05h	[7:0]									
3D0Ch	[0]	INCKSEL6	1h							
3D18h	[7:0]	TCLKPOST	00B7h	0067h	0067h	006Fh	009Fh	009Fh	00B7h	Global timing
3D19h	[7:0]									
3D1Ah	[7:0]	TCLKPREPARE	0067h	0027h	0027h	002Fh	0057h	0057h	0067h	Global timing
3D1Bh	[7:0]									
3D1Ch	[7:0]	TCLKTRAIL	006Fh	0027h	0027h	002Fh	0057h	0057h	006Fh	Global timing
3D1Dh	[7:0]									
3D1Eh	[7:0]	TCLKZERO	01DFh	00B7h	00B7h	00BFh	0187h	0187h	01DFh	Global timing
3D1Fh	[7:0]									
3D20h	[7:0]	THSPREPARE	006Fh	002Fh	002Fh	002Fh	005Fh	005Fh	006Fh	Global timing
3D21h	[7:0]									
3D22h	[7:0]	THSZERO	00CFh	004Fh	004Fh	0057h	00A7h	00A7h	00CFh	Global timing
3D23h	[7:0]									
3D24h	[7:0]	THSTRAIL	006Fh	002Fh	002Fh	002Fh	005Fh	005Fh	006Fh	Global timing
3D25h	[7:0]									
3D26h	[7:0]	THSEXIT	00B7h	0047h	0047h	004Fh	0097h	0097h	00B7h	Global timing
3D27h	[7:0]									
3D28h	[7:0]	TLPX	005Fh	0027h	0027h	0027h	004Fh	004Fh	005Fh	Global timing
3D29h	[7:0]									

Address	bit	Register Name	Initial Value	CSI-2 serial / 8lane					Remark
				30	60	30	60	90.1	[frame/s]
				594	720		891	1188	[Mbps/lane]
				14.8	7.4	14.8	7.4	4.9	1H period[μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	Refer to “INCK setting”					
3009h	[1:0]								
300Ah	[7:0]	CPWAIT_TIME	0B6h						
300Bh	[1:0]								
	[7:4]	EFWAIT_TIME	Ah						
301Ch	[3:0]	WINMODE	0h	0h					All pixel mode
3022h	[1:0]	ADDMODE	0h	0h					All pixel mode
3024h	[7:0]	VMAX	8CAh	8CAh					
3025h	[7:0]								
3026h	[3:0]								
3028h	[7:0]	HMAX	226h	44Ch	226h	44Ch	226h	16Eh	
3029h	[7:0]								
3030h	[0]	HREVERSE	0h	0h / 1h					0: Nor, 1: Inv
	[1]	VREVERSE	0h	0h / 1h					0: Nor, 1: Inv
3031h	[1:0]	ADBIT	1h	0h	0h	1h	1h	0h	0: 10 bit, 1: 12 bit
3032h	[0]	MDBIT	1h	0h	0h	1h	1h	0h	0: 10 bit, 1: 12 bit
3114h	[7:0]	INCKSEL1	00h	Refer to “INCK setting”					
3119h	[7:0]	INCKSEL2	28h						
311Ch	[7:0]	INCKSEL3	0C0h						
311Dh	[0]								
3152h to 37FFh	[7:0]	Refer to “Register Map”							
3804h	[1:0]	INCKSEL4	3h	Refer to “INCK setting”					
3807h	[7:0]	INCKSEL5	60h						
3888h to 3AFFh	[7:0]	Refer to “Register Map”							

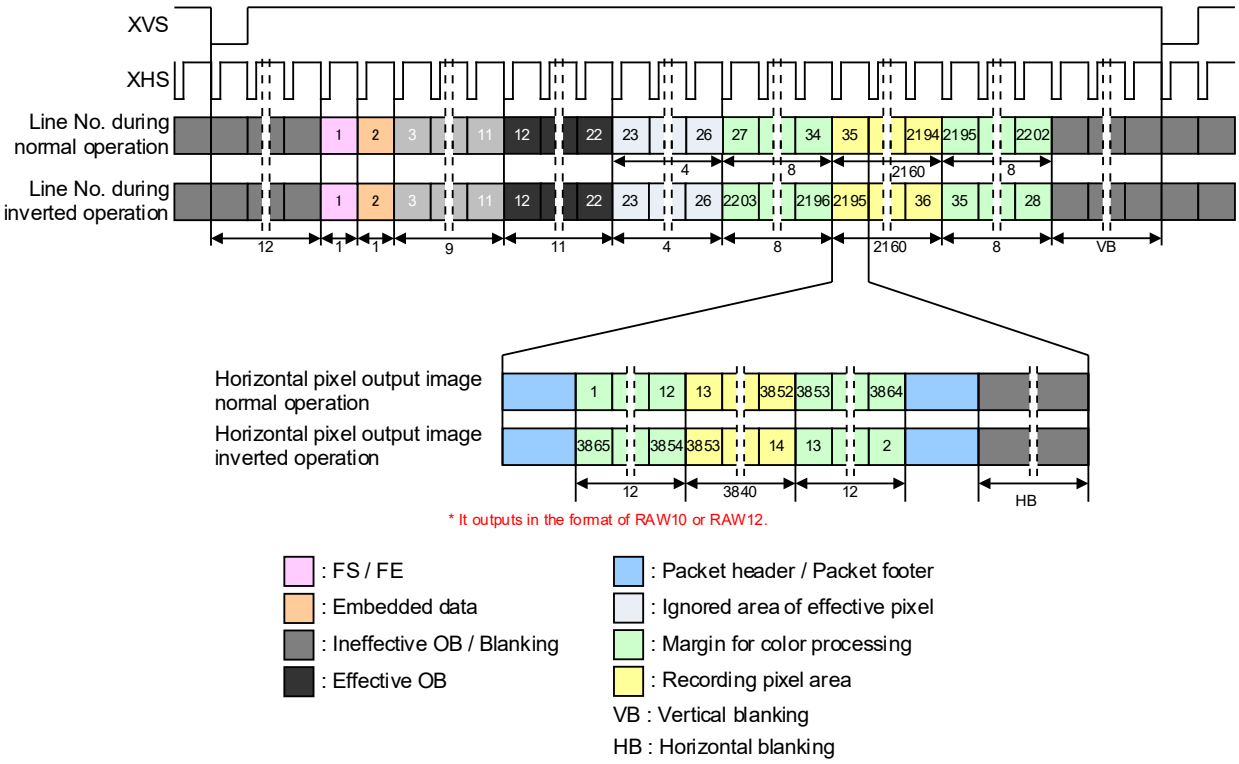
Address	bit	Register Name	Initial Value	CSI-2 serial / 8lane					Remark
				30	60	30	60	90.1	[frame/s]
				594	720		891	1188	[Mbps/lane]
3D01h	[2:0]	LANEMODE	3h	7h					8Lane
3D04h	[7:0]	TXCLCKES_FREQ	1290h	Refer to “INCK setting”					
3D05h	[7:0]								
3D0Ch	[0]	INCKSEL6	1h						
3D18h	[7:0]	TCLKPOST	00B7h	0067h	006Fh	006Fh	007Fh	008Fh	Global timing
3D19h	[7:0]								
3D1Ah	[7:0]	TCLKPREPARE	0067h	0027h	002Fh	002Fh	0037h	004Fh	Global timing
3D1Bh	[7:0]								
3D1Ch	[7:0]	TCLKTRAIL	006Fh	0027h	002Fh	002Fh	0037h	0047h	Global timing
3D1Dh	[7:0]								
3D1Eh	[7:0]	TCLKZERO	01DFh	00B7h	00BFh	00BFh	00F7h	0137h	Global timing
3D1Fh	[7:0]								
3D20h	[7:0]	THSPREPARE	006Fh	002Fh	002Fh	002Fh	003Fh	004Fh	Global timing
3D21h	[7:0]								
3D22h	[7:0]	THSZERO	00CFh	004Fh	0057h	0057h	006Fh	0087h	Global timing
3D23h	[7:0]								
3D24h	[7:0]	THSTRAIL	006Fh	002Fh	002Fh	002Fh	003Fh	004Fh	Global timing
3D25h	[7:0]								
3D26h	[7:0]	THSEXIT	00B7h	0047h	004Fh	004Fh	005Fh	007Fh	Global timing
3D27h	[7:0]								
3D28h	[7:0]	TLPX	005Fh	0027h	0027h	0027h	002Fh	003Fh	Global timing
3D29h	[7:0]								

Address	bit	Register Name	Initial Value	CSI-2 serial / 4lane × 2ch					Remark
				30	60	30	60	90.1	[frame/s]
				594	891		1188		[Mbps/lane]
				14.8	7.4	14.8	7.4	4.9	1H period[μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	Refer to “INCK setting”					
3009h	[1:0]								
300Ah	[7:0]	CPWAIT_TIME	0B6h						
300Bh	[1:0]								
	[7:4]	EFWAIT_TIME	Ah						
301Ch	[3:0]	WINMODE	0h	0h					All pixel mode
3022h	[1:0]	ADDMODE	0h	0h					All pixel mode
3024h	[7:0]	VMAX	8CAh	8CAh					
3025h	[7:0]								
3026h	[3:0]								
3028h	[7:0]	HMAX	226h	44Ch	226h	44Ch	226h	16Eh	
3029h	[7:0]								
3030h	[0]	HREVERSE	0h	0h / 1h					0: Nor, 1: Inv
	[1]	VREVERSE	0h	0h / 1h					0: Nor, 1: Inv
3031h	[1:0]	ADBIT	1h	0h	0h	1h	0h	1h	0: 10 bit, 1: 12 bit
3032h	[0]	MDBIT	1h	0h	0h	1h	0h	1h	0: 10 bit, 1: 12 bit
3040h	[7:0]	XSIZE_OVERLAP	000h	03Ch					
3041h	[2:0]								
3114h	[7:0]	INCKSEL1	00h	Refer to “INCK setting”					
3119h	[7:0]	INCKSEL2	28h						
311Ch	[7:0]	INCKSEL3	0C0h						
311Dh	[0]								
3152h to 37FFh	[7:0]	Refer to “Register Map”							
3804h	[1:0]	INCKSEL4	3h	Refer to “INCK setting”					
3807h	[7:0]	INCKSEL5	60h						
3888h to 3AFFh	[7:0]	Refer to “Register Map”							

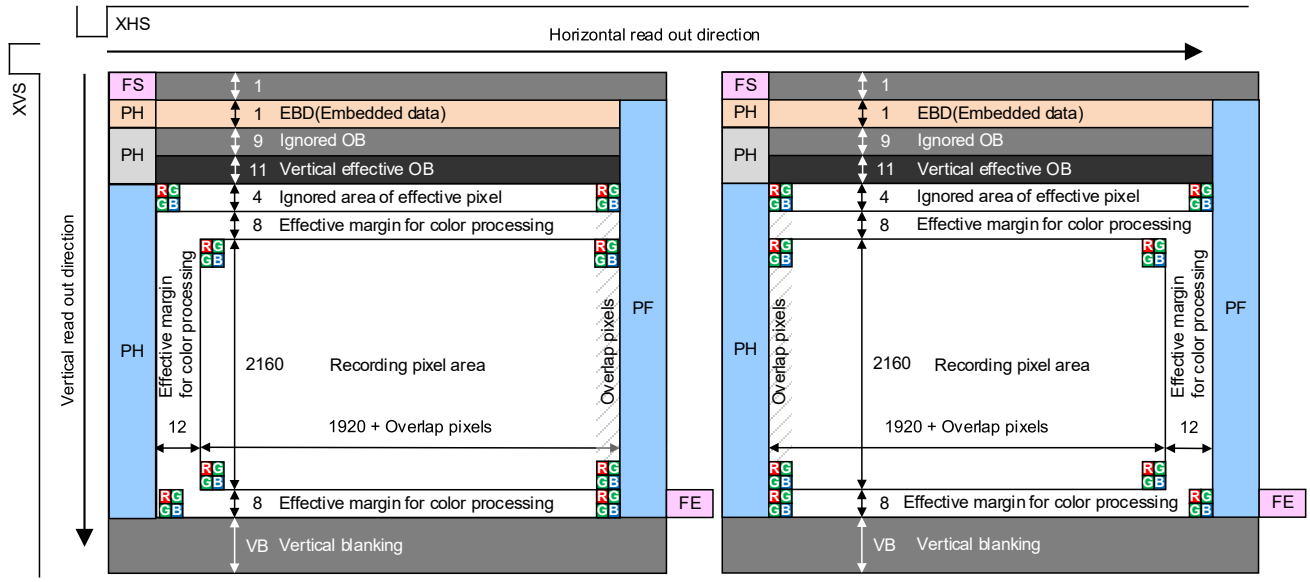
Address	bit	Register Name	Initial Value	CSI-2 serial / 4lane × 2ch					Remark
				30	60	30	60	90.1	[frame/s]
				594	891		1188		[Mbps/lane]
3D01h	[2:0]	LANEMODE	3h	6h					4Lane × 2ch
3D04h	[7:0]	TXCLCKES_FREQ	1290h	Refer to “INCK setting”					
3D05h	[7:0]								
3D0Ch	[0]	INCKSEL6	1h						
3D18h	[7:0]	TCLKPOST	00B7h	0067h	007Fh	007Fh	008Fh	008Fh	Global timing
3D19h	[7:0]								
3D1Ah	[7:0]	TCLKPREPARE	0067h	0027h	0037h	0037h	004Fh	004Fh	Global timing
3D1Bh	[7:0]								
3D1Ch	[7:0]	TCLKTRAIL	006Fh	0027h	0037h	0037h	0047h	0047h	Global timing
3D1Dh	[7:0]								
3D1Eh	[7:0]	TCLKZERO	01DFh	00B7h	00F7h	00F7h	0137h	0137h	Global timing
3D1Fh	[7:0]								
3D20h	[7:0]	THSPREPARE	006Fh	002Fh	003Fh	003Fh	004Fh	004Fh	Global timing
3D21h	[7:0]								
3D22h	[7:0]	THSZERO	00CFh	004Fh	006Fh	006Fh	0087h	0087h	Global timing
3D23h	[7:0]								
3D24h	[7:0]	THSTRAIL	006Fh	002Fh	003Fh	003Fh	004Fh	004Fh	Global timing
3D25h	[7:0]								
3D26h	[7:0]	THSEXIT	00B7h	0047h	005Fh	005Fh	007Fh	007Fh	Global timing
3D27h	[7:0]								
3D28h	[7:0]	TLPX	005Fh	0027h	002Fh	002Fh	003Fh	003Fh	Global timing
3D29h	[7:0]								



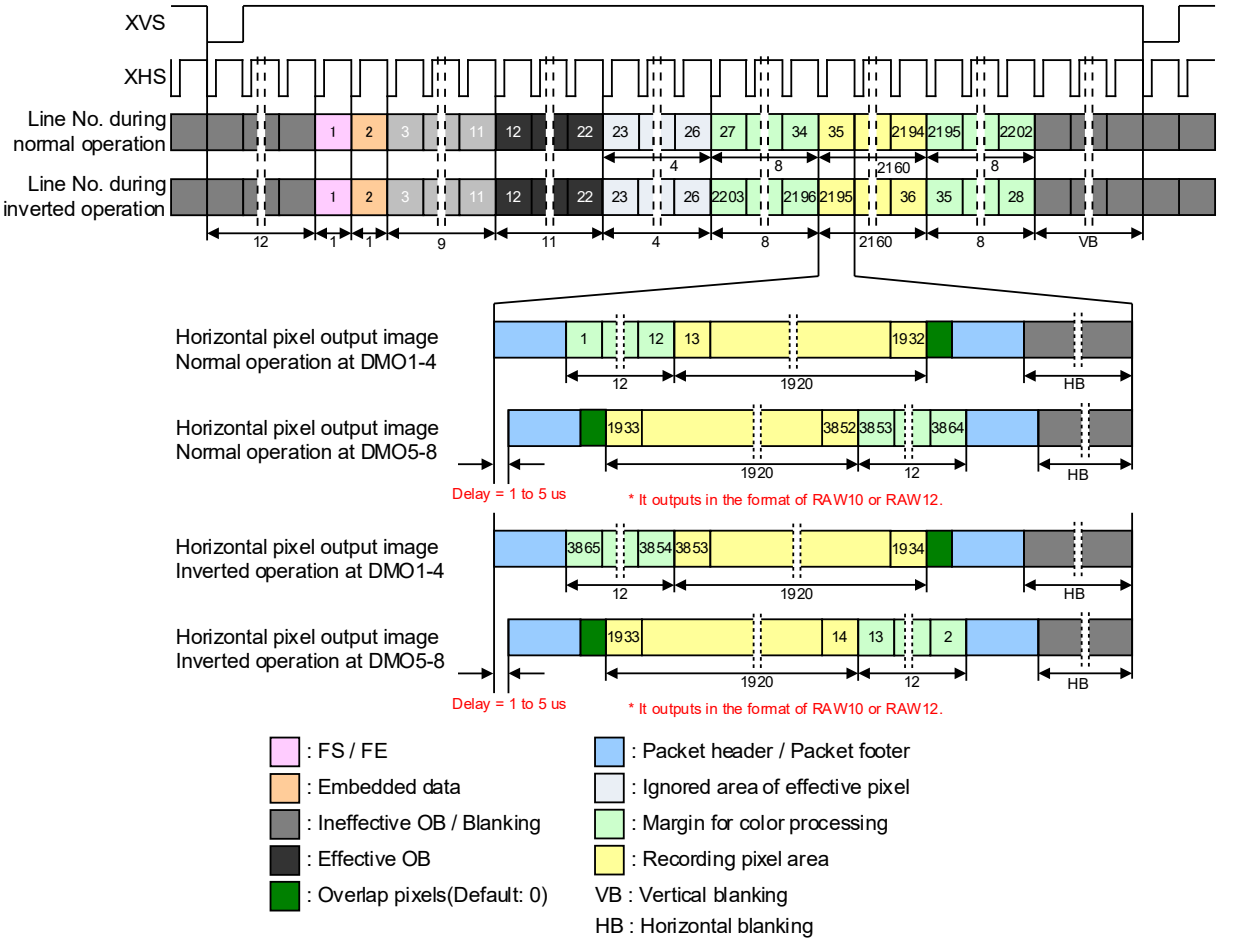
Pixel Array Image Drawing in All pixel mode (2,4,8 Lanes)



Drive Timing Chart for All pixel mode (2,4,8 Lanes)



Pixel Array Image Drawing in All pixel mode (4 Lane × 2ch)



Drive Timing Chart for All pixel mode (4 Lane × 2ch)

Horizontal/Vertical 2/2-line binning mode

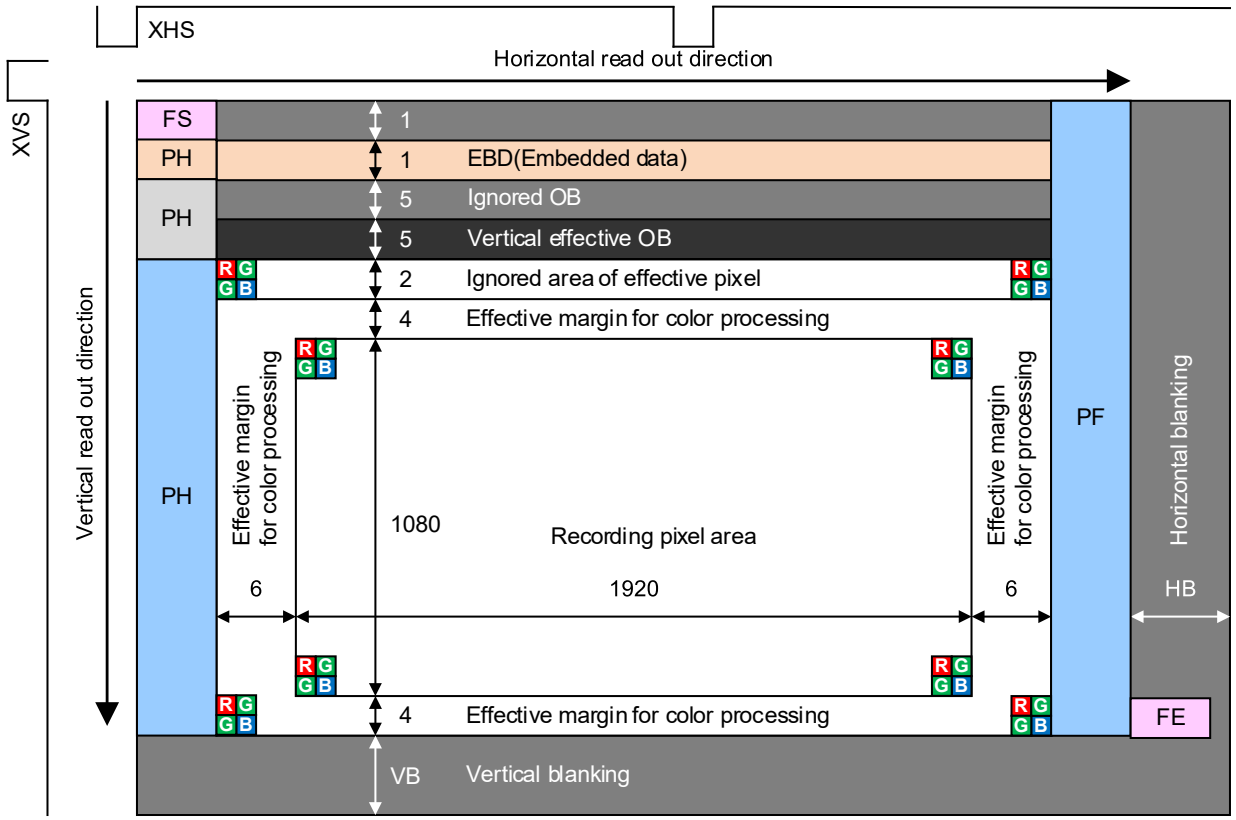
List of Setting Register

Address	bit	Register Name	Initial Value	CSI-2 serial / 2lane	CSI-2 serial / 4lane			Remark
				30	30	30	60	[frame/s]
				1440	594	720	1440	[Mbps/lane]
				14.8	14.8	14.8	7.4	1H period[μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	Refer to “INCK setting”				
3009h	[1:0]							
300Ah	[7:0]	CPWAIT_TIME	0B6h					
300Bh	[1:0]							
	[7:4]	EFWAIT_TIME	Ah					
301Ch	[3:0]	WINMODE	0h	0h				All pixel mode
3020h	[0]	HADD	0h	1h				Horizontal 2 binning
3021h	[0]	VADD	0h	1h				Vertical 2 binning
3022h	[1:0]	ADDMODE	0h	1h				H/V 2/2-line binning
3024h	[7:0]	VMAX	8CAh	8CAh				
3025h	[7:0]							
3026h	[3:0]							
3028h	[7:0]	HMAX	226h	44Ch			226h	
3029h	[7:0]							
3030h	[0]	HREVERSE	0h	0h / 1h				0: Nor. , 1: Inv.
	[1]	VREVERSE	0h	0h / 1h				0: Nor. , 1: Inv.
3031h	[1:0]	ADBIT	1h	0h				10 bit
3032h	[0]	MDBIT	1h	1h				12 bit
30D5h	[4:0]	DIG_CLP_VSTART	04h	02h				
3114h	[7:0]	INCKSEL1	00h	Refer to “INCK setting”				
3119h	[7:0]	INCKSEL2	28h					
311Ch	[7:0]	INCKSEL3	0C0h					
311Dh	[2:0]							
3152h to 37FFh	[7:0]	Refer to “Register Map setting”						
3804h	[1:0]	INCKSEL4	3h	Refer to “INCK setting”				
3807h	[7:0]	INCKSEL5	60h					
3888h to 3AFFh	[7:0]	Refer to “Register Map setting”						

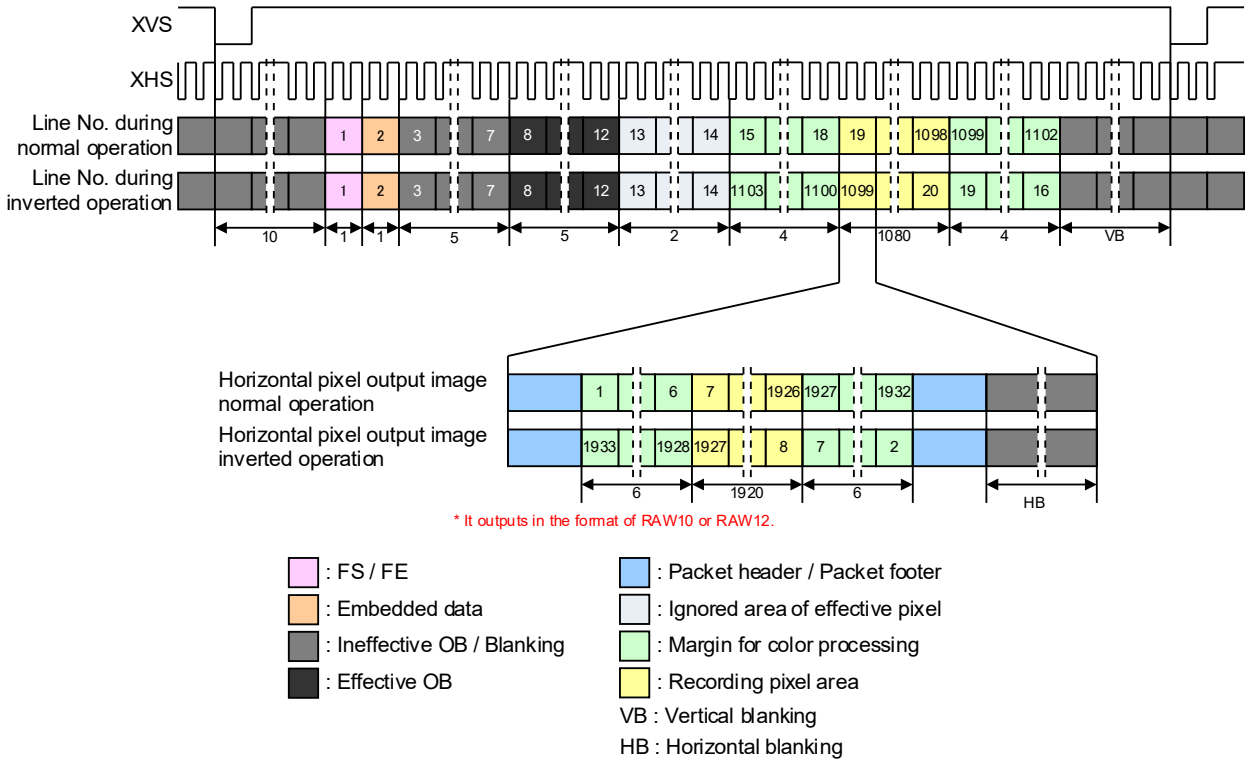
Address	bit	Register Name	Initial Value	CSI-2 serial / 2lane	CSI-2 serial / 4lane			Remark
				30	30	30	60	[frame/s]
				1440	594	720	1440	[Mbps/lane]
3D01h	[2:0]	LANEMODE	3h	1h	3h			1: 2Lane 3: 4Lane
3D04h	[7:0]	TXCLCKES_FREQ	1290h	Refer to “INCK setting”				
3D05h	[7:0]							
3D0Ch	[0]	INCKSEL6	1h					
3D18h	[7:0]	TCLKPOST	00B7h	009Fh	0067h	006Fh	009Fh	Global timing
3D19h	[7:0]							
3D1Ah	[7:0]	TCLKPREPARE	0067h	0057h	0027h	002Fh	0057h	Global timing
3D1Bh	[7:0]							
3D1Ch	[7:0]	TCLKTRAIL	006Fh	0057h	0027h	002Fh	0057h	Global timing
3D1Dh	[7:0]							
3D1Eh	[7:0]	TCLKZERO	01DFh	0187h	00B7h	00BFh	0187h	Global timing
3D1Fh	[7:0]							
3D20h	[7:0]	THSPREPARE	006Fh	005Fh	002Fh	002Fh	005Fh	Global timing
3D21h	[7:0]							
3D22h	[7:0]	THSZERO	00CFh	00A7h	004Fh	0057h	00A7h	Global timing
3D23h	[7:0]							
3D24h	[7:0]	THSTRAIL	006Fh	005Fh	002Fh	002Fh	005Fh	Global timing
3D25h	[7:0]							
3D26h	[7:0]	THSEXIT	00B7h	0097h	0047h	004Fh	0097h	Global timing
3D27h	[7:0]							
3D28h	[7:0]	TLPX	005Fh	004Fh	0027h	0027h	004Fh	Global timing
3D29h	[7:0]							

Address	bit	Register Name	Initial Value	CSI-2 serial / 8lane			CSI-2 serial / 4lane × 2ch			Remark
				30	60	90.1	30	60	90.1	[frame/s]
				594	720	1188	594	891	1440	[Mbps/lane]
				14.8	7.4	4.9	14.8	7.4	4.9	1H period[μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	Refer to “INCK setting”						
3009h	[1:0]									
300Ah	[7:0]	CPWAIT_TIME	0B6h							
300Bh	[1:0]									
	[7:4]	EFWAIT_TIME	Ah							
301Ch	[3:0]	WINMODE	0h	0h						All pixel mode
3020h	[0]	HADD	0h	1h						Horizontal 2 binning
3021h	[0]	VADD	0h	1h						Vertical 2 binning
3022h	[1:0]	ADDMODE	0h	1h						H/V 2/2-line binning
3024h	[7:0]	VMAX	8CAh	8CAh						
3025h	[7:0]									
3026h	[3:0]									
3028h	[7:0]	HMAX	226h	44Ch	224h	16Eh	44Ch	224h	16Eh	
3029h	[7:0]									
3030h	[0]	HREVERSE	0h	0h / 1h						0: Nor. , 1: Inv.
	[1]	VREVERSE	0h	0h / 1h						0: Nor. , 1: Inv.
3031h	[1:0]	ADBIT	1h	0h						10 bit
3032h	[0]	MDBIT	1h	1h						12 bit
3040h	[7:0]	XSIZE_OVERLAP	000h	000h			03Ch			
3041h	[2:0]									
30D5h	[4:0]	DIG_CLP_VSTART	04h	02h						
3114h	[7:0]	INCKSEL1	00h	Refer to “INCK setting”						
3119h	[7:0]	INCKSEL2	28h							
311Ch	[7:0]	INCKSEL3	0C0h							
311Dh	[2:0]									
3152h to 37FFh	[7:0]	Refer to “Register Map setting”								
3804h	[1:0]	INCKSEL4	3h	Refer to “INCK setting”						
3807h	[7:0]	INCKSEL5	60h							
3888h to 3AFFh	[7:0]	Refer to “Register Map setting”								

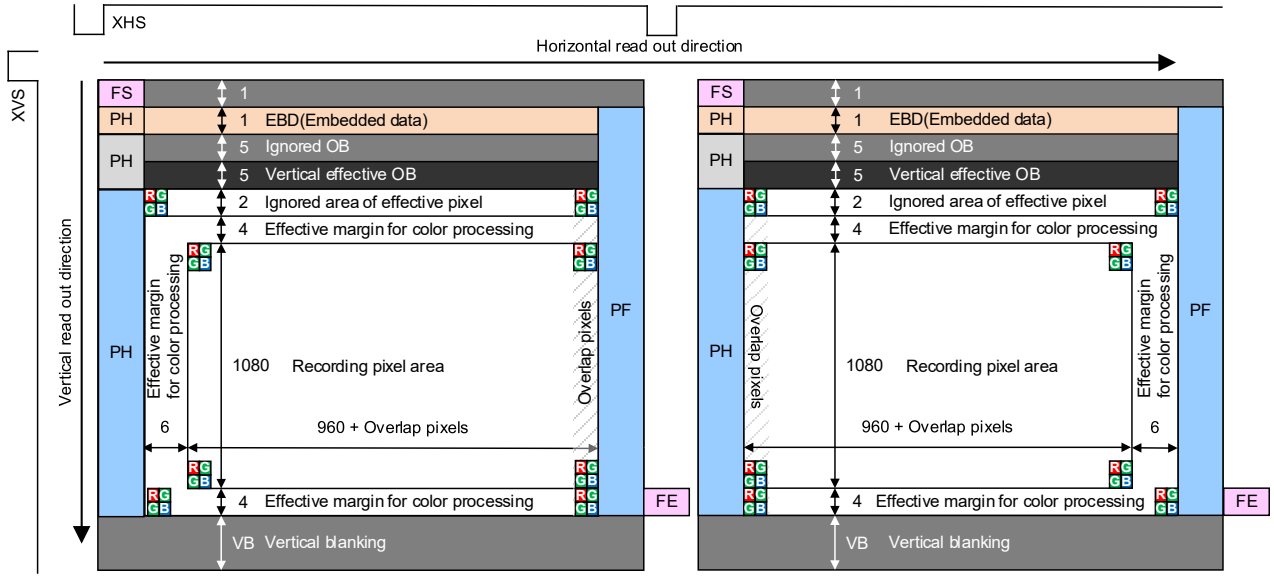
Address	bit	Register Name	Initial Value	CSI-2 serial / 8lane			CSI-2 serial / 4lane × 2ch			Remark
				30	60	90.1	30	60	90.1	[frame/s]
				594	720	1188	594	891	1440	[Mbps/lane]
3D01h	[2:0]	LANEMODE	3h	7h			6h			7: 8Lane 6: 4Lane × 2ch
3D04h	[7:0]	TXCLCKES_FREQ	1290h	Refer to “INCK setting”						
3D05h	[7:0]									
3D0Ch	[0]	INCKSEL6	1h							
3D18h	[7:0]	TCLKPOST	00B7h	0067h	006Fh	008Fh	0067h	007Fh	009Fh	Global timing
3D19h	[7:0]									
3D1Ah	[7:0]	TCLKPREPARE	0067h	0027h	002Fh	004Fh	0027h	0037h	0057h	Global timing
3D1Bh	[7:0]									
3D1Ch	[7:0]	TCLKTRAIL	006Fh	0027h	002Fh	0047h	0027h	0037h	0057h	Global timing
3D1Dh	[7:0]									
3D1Eh	[7:0]	TCLKZERO	01DFh	00B7h	00BFh	0137h	00B7h	00F7h	0187h	Global timing
3D1Fh	[7:0]									
3D20h	[7:0]	THSPREPARE	006Fh	002Fh	002Fh	004Fh	002Fh	003Fh	005Fh	Global timing
3D21h	[7:0]									
3D22h	[7:0]	THSZERO	00CFh	004Fh	0057h	0087h	004Fh	006Fh	00A7h	Global timing
3D23h	[7:0]									
3D24h	[7:0]	THSTRAIL	006Fh	002Fh	002Fh	004Fh	002Fh	003Fh	005Fh	Global timing
3D25h	[7:0]									
3D26h	[7:0]	THSEXIT	00B7h	0047h	004Fh	007Fh	0047h	005Fh	0097h	Global timing
3D27h	[7:0]									
3D28h	[7:0]	TLPX	005Fh	0027h	0027h	003Fh	0027h	002Fh	004Fh	Global timing
3D29h	[7:0]									



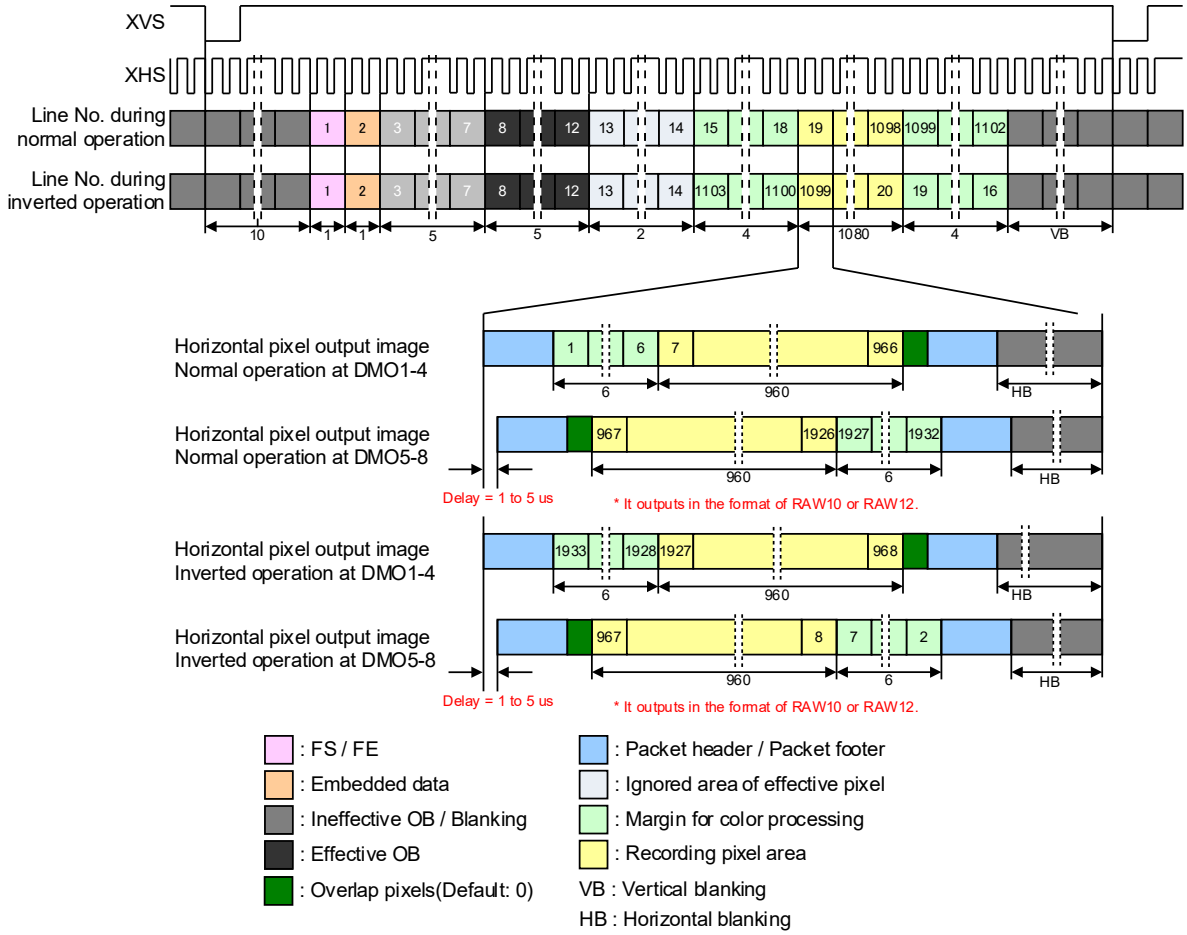
Pixel Array Image Drawing in Horizontal /Vertical 2/2-line binning mode (2,4,8 Lanes)



Drive Timing Chart for Horizontal /Vertical 2/2-line binning mode (2,4,8 Lanes)



Pixel Array Image Drawing in Horizontal /Vertical 2/2-line binning mode (4 Lane × 2ch)



Drive Timing Chart for Horizontal /Vertical 2/2-line binning mode (4 Lane × 2ch)

Window Cropping Mode

Sensor signals are cut out and read out in arbitrary positions.
This function support All-pixel mode, Horizontal/Vertical 2/2-line binning mode, Multiple exposure HDR, Digital overlap HDR and Vertical / Horizontal direction-normal / inverted readout mode of each modes.

Cropping position is set, regarding effective pixel start position as origin (0, 0) in normal mode direction. That is a start point which is an offset from the origin and cropping width.
Cropping is available from all-pixel scan mode and horizontal period is fixed to the value for this mode. Pixels cropped by horizontal cropping setting are output with left shifted and that extends the horizontal blanking period.
Window position and size is used fixed value. (An ignore frame is output when it is changed.)

Window cropping image is shown in the figure below.
The same physical pixel area as all-pixel mode is cropped when start position and width are same setting in Horizontal/Vertical 2/2-line binning mode, Multiple exposure HDR, Digital overlap HDR and Vertical / Horizontal direction-normal / inverted readout mode.
At inverted mode, it is the same as the “Recording pixel with Effective margin for color processing (green rectangle in the figure) “ area in normal mode.

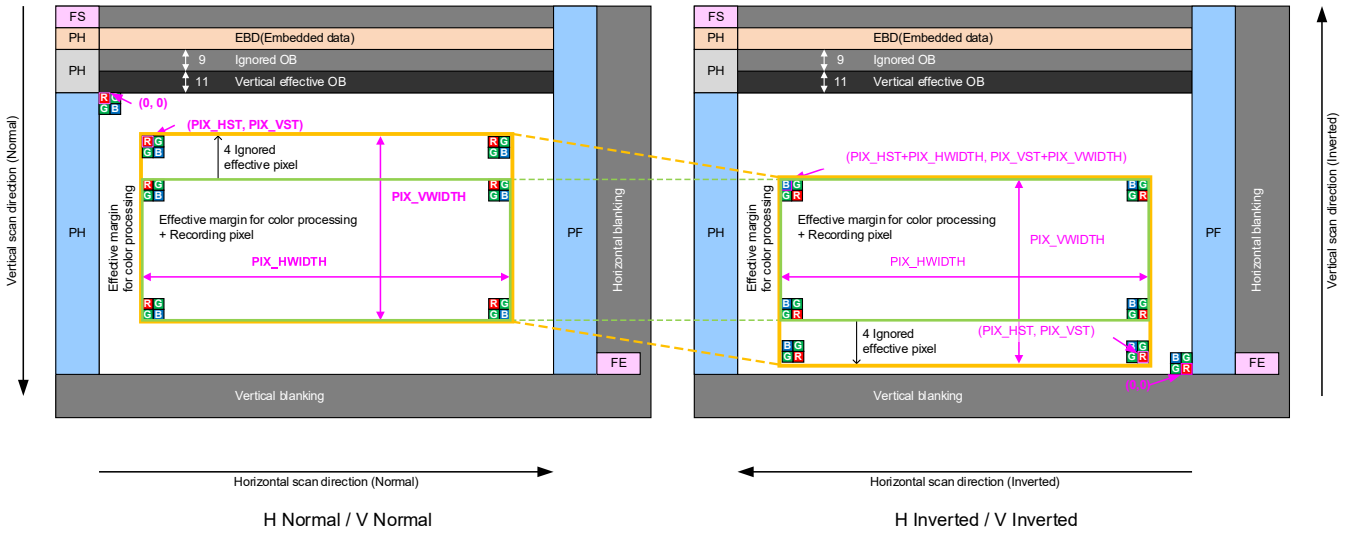


Image Drawing of Window Cropping Mode in Horizontal/Vertical, normal/inverted direction

List of Setting Register

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
WINMODE	301Ch	[3:0]	0h	4h: Window Cropping mode	-
PIX_HST	303Ch	[7:0]	0000h	Effective pixel Start position (Horizontal direction)	Non-binning : multiple of 2 Horizontal/Vertical 2/2-line binning : multiple of 2
	303Dh	[4:0]			
PIX_HWIDTH	303Eh	[7:0]	0F18h	Effective pixel Cropping width (Horizontal direction)	Non-binning : multiple of 12 Horizontal /Vertical 2/2-line binning : multiple of 24
	303Fh	[4:0]			
PIX_VST	3044h	[7:0]	0000h	Effective pixel Start position (Vertical direction)	Non-binning : multiple of 2 Horizontal/Vertical 2/2-line binning : multiple of 4
	3045h	[4:0]			
PIX_VWIDTH	3046h	[7:0]	0884h	Effective pixel Cropping width (Vertical direction)	Non-binning : multiple of 2 Horizontal/Vertical 2/2-line binning : multiple of 4
	3047h	[4:0]			

Restrictions on Window cropping mode
The register settings should satisfy following conditions:

Set WINMODE: 4h.

◆ PIX_VST, PIX_VWIDTH

About non-binning, Set PIX_VST, PIX_VWIDTH to a multiple of 2.

$PIX\_VST = n_1 \times 2$
$PIX\_VWIDTH = n_2 \times 2$

About Horizontal/Vertical 2/2-line binning, Set PIX_VST, PIX_VWIDTH to a multiple of 4.

$PIX\_VST = n_1 \times 4$
$PIX\_VWIDTH = n_2 \times 4$

Cropped area is needed to set pre 4 pixel, rear 0 pixel for signal processing.

◆ PIX_HST, PIX_HWIDTH

About non-binning

Set PIX_HST to a multiple of 2.
Set PIX_HWIDTH to a multiple of 12.

$PIX\_HST = n_3 \times 2$
$PIX\_VWIDTH = n_4 \times 12$

About About Horizontal/Vertical 2/2-line binning

Set PIX_HST to a multiple of 2.
Set PIX_HWIDTH to a multiple of 24.

$PIX\_HST = n_3 \times 2$
$PIX\_VWIDTH = n_4 \times 24$

Where $n_{1\sim4}$ are integer equal or more than 0.

V_{TTL} (1farame line length or VMAX) ≥ PIX_VWIDTH + 70
Set V_{TTL} to 1106 or more.

$$V_{TTL} \geq 1106$$

◆ Frame rate on Window cropping mode

Frame rate [frame/s] = 1 / (V_{TTL} × (1H period))
1H period (unit: [μs]) : Fix 1H time in a mode before cropping and refer to the value of "1H period" in the table of "Operating Mode".

Where V_{TTL} is 1frame line length or VMAX.

Description of Various Function

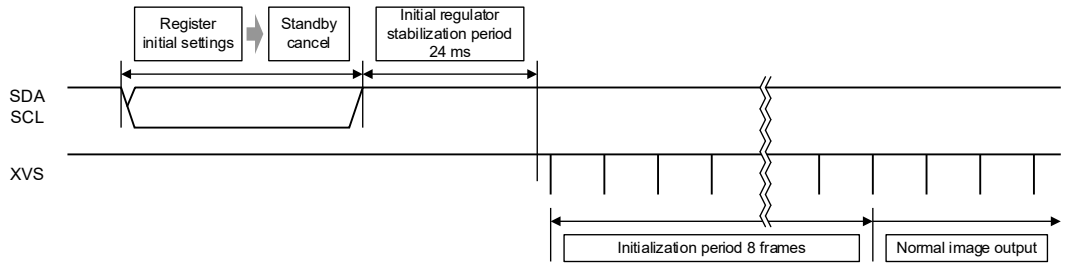
Standby Mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

List of Standby Mode Setting

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
STANDBY	3000h	[0]	1h	1h: Standby 0h: Operating	Register communication is executed in standby mode.

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. After standby mode is canceled, a normal image is output from the 8 frames after internal regulator stabilization 24 ms or more.
For details of the sequence of setting and cancel standby mode, see the sensor setting flow after power on.



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this register status during operation.)

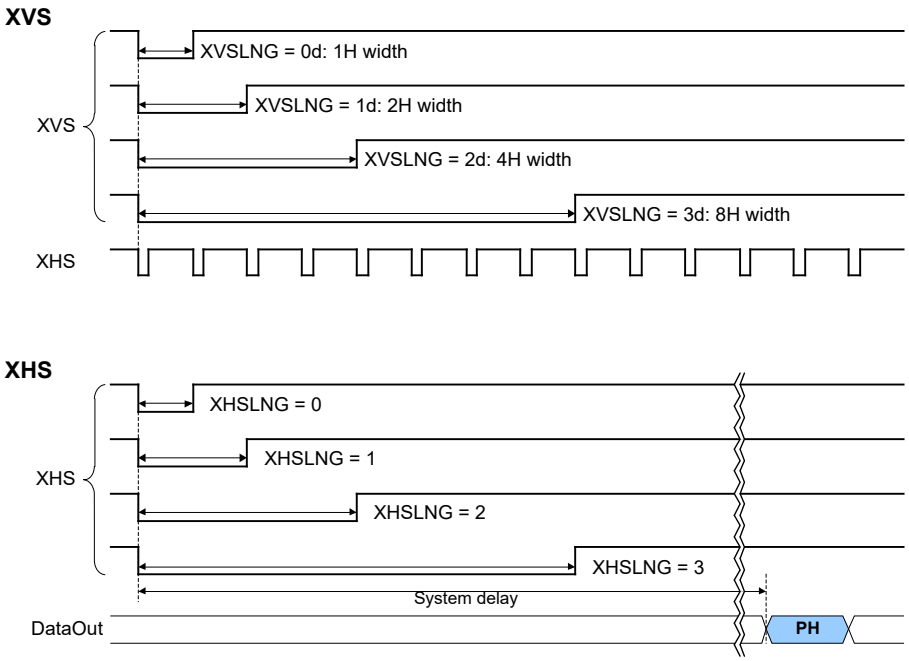
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Operating mode" for the number of output data line and 1H period.
Set the XMSTA register 0h in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [19:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of Operation Mode for details of the section of “Operating Modes”.

List of Slave and Master Mode Setting

Pin name	Pin processing	Setting value	Remarks
XMASTER pin	Fixed to Low	Master mode	High: OV_{DD}
	Fixed to High	Slave mode	Low: GND

List of Register in Master Mode

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
XMSTA	3002h	[0]	1h	1h: Master operation ready 0h: Master operation start	The master operation starts by setting 0.
VMAX [19:0]	3024h	[7:0]	008CAh	See the item of each drive mode.	Line number per frame designated * Set value multiple of 2
	3025h	[7:0]			
	3026h	[3:0]			
HMAX [15:0]	3028h	[7:0]	0226h	See the item of each drive mode.	Clock number per line designated
	3029h	[7:0]			
XVSOUTSEL [1:0]	30A4h	[1:0]	2h	0h: Fixed to Low 2h: VSYNC output	
XHSOUTSEL [1:0]		[3:2]	2h	0h: Fixed to Low 2h: HSYNC output	
XVS_DRV [1:0]	30A5h	[1:0]	3h	0h: XVS output (Master mode) 3h: Hi-z (Slave mode)	
XHS_DRV [1:0]		[3:2]	3h	0h: XHS output (Master mode) 3h: Hi-z (Slave mode)	
XVSLNG [1:0]	30CCh	[5:4]	0h	0h: 1H, 1h: 2H, 2h: 4H, 3h: 8H	XVS low level pulse width designated
XHSLNG [1:0]	30CDh	[6:5]	0h	0h: 16clock, 1h: 32clock 2h: 64clock, 3h: 128clock See the next	XHS low level pulse width designated



XVS/XHS output waveform in sensor master mode

The XVS and XHS are output in timing that set 0 to the register XMSTA. If set 0 to XMSTA during standby, the XVS and XHS are output just after standby is released. The XVS and XHS are output asynchronous with other input or output signals. In addition, the output signals are output with an undefined latency time (system delay) relative to the XHS. Therefore, refer to the sync codes output from the sensor and perform synchronization.

Gain Adjustment Function

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block. The total of analog gain and digital gain can be set up to 72dB by the GAIN [10:0] register setting. The same setting is applied in all colors.

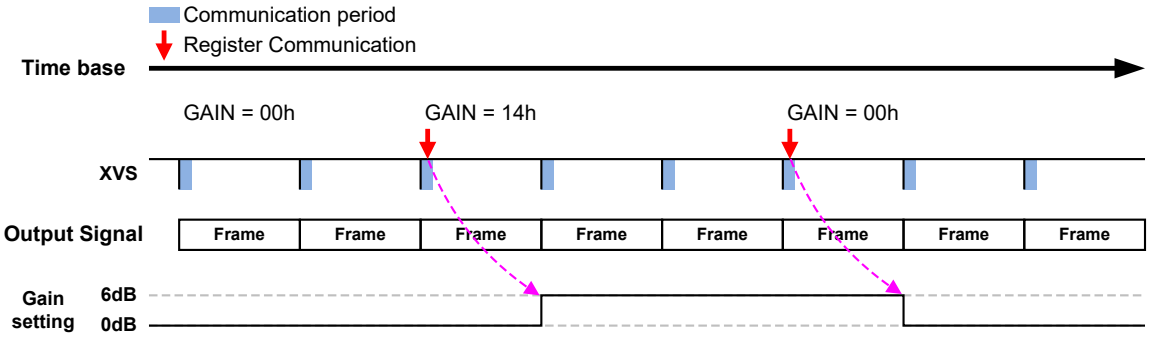
The value which is 10/3 times the gain is set to register. (0.3 dB step)

Example)
When set to 6 dB: 6 × 10/3 = 20d; GAIN = 14h
When set to 12.6 dB: 12.6 × 10/3 = 42d; GAIN = 2Ah

List of PGC Register

Register	Register details		Initial value	Setting value	Remarks
	Address	bit		Setting range	
GAIN [10:0]	3084h	[7:0]	000h	00h-F0h (0d-240d)	Setting value: Gain [dB] × 10/3 (0.3 dB step)
	3085h	[2:0]			

The gain setting is reflected at the next frame that the communication is performed as shown below.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 3FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [9:0] register.
Note that the offset unit changes according to the output bit setting.
When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 LSB. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 LSB.

Use with values shown below is recommended.
10-bit output: 032h (50d)
12-bit output: 032h (200d)

List of Black Level Adjustment Register

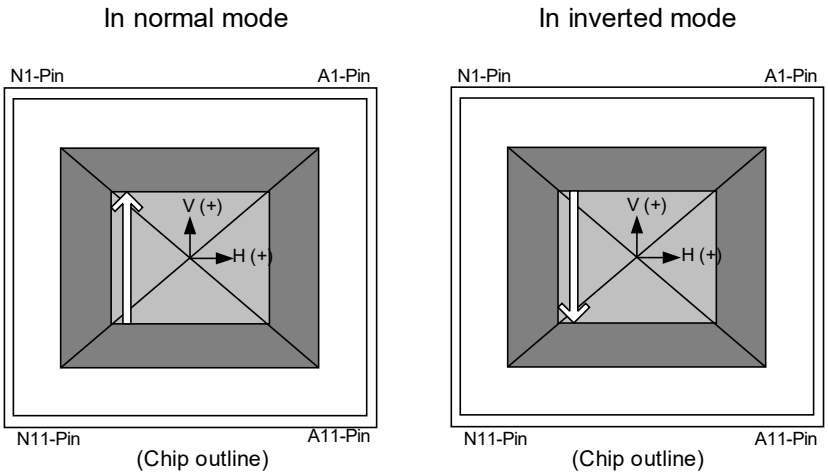
Register	Register details		Initial value	Setting value
	Address	bit		
BLKLEVEL [9:0]	30DCh	[7:0]	032h	000h to 3FFh
	30DDh	[1:0]		

Normal Operation and Inverted Operation

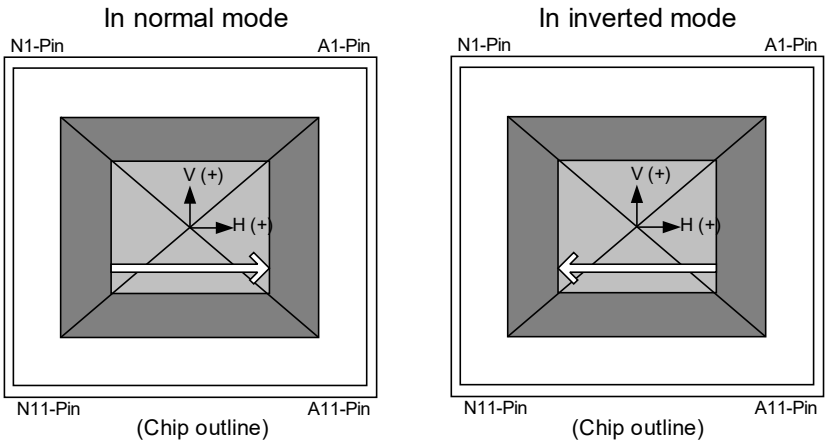
The sensor readout direction (normal / inverted) in vertical direction can be switched by VREVERSE register settings and in horizontal direction can be switched by the HREVERSE register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes. See the section of “List of Setting Register” for the other register settings.
One invalid frame is generated when reading immediately after the readout vertical direction change in order to switch the normal operation and inversion between frames.

List of Drive Direction Setting Register

Register	Register details		Initial value	Setting value
	Address	bit		
HREVERSE	3030h	[0]	0h	0h: Normal 1h: Inverted
VREVERSE		[1]	0h	0h: Normal 1h: Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - SHR0 × (1H period)

*1 The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
*2 See “Operating Modes” for the 1H period.
*3 Set multiple of 2 about the time of SHR0.

In this section, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

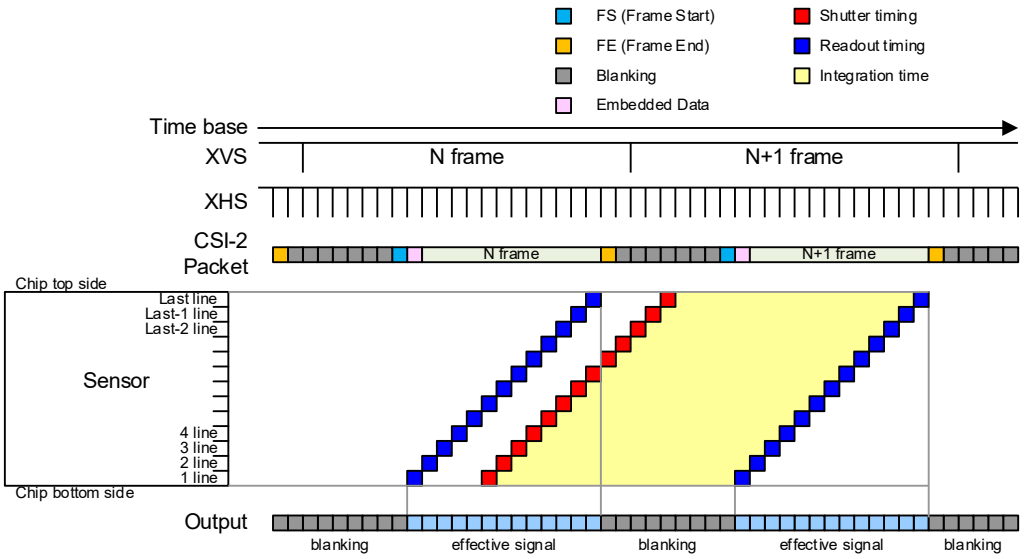


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 2H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHR0 [19:0] register. Set SHR0 [19:0] to a value between 8 and (Number of lines per frame - 4). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit.
When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX register. The number of lines per frame differs according to the operating mode.

Registers Used to Set the Integration Time in 2H Units

Register	Register details		Initial value	Setting value
	Address	bit		
SHR0 [19:0]	3050h	[7:0]	00006h	Sets the shutter sweep time. 6 to (Number of lines per frame - 2) * Others: Setting prohibited * Set value multiple of 2
	3051h	[7:0]		
	3052h	[3:0]		
VMAX [19:0]	3024h	[7:0]	008CAh	Sets the number of lines per frame (only in master mode). See “Operating Modes” for the setting value in each mode. * Set value multiple of 2
	3025h	[7:0]		
	3026h	[3:0]		

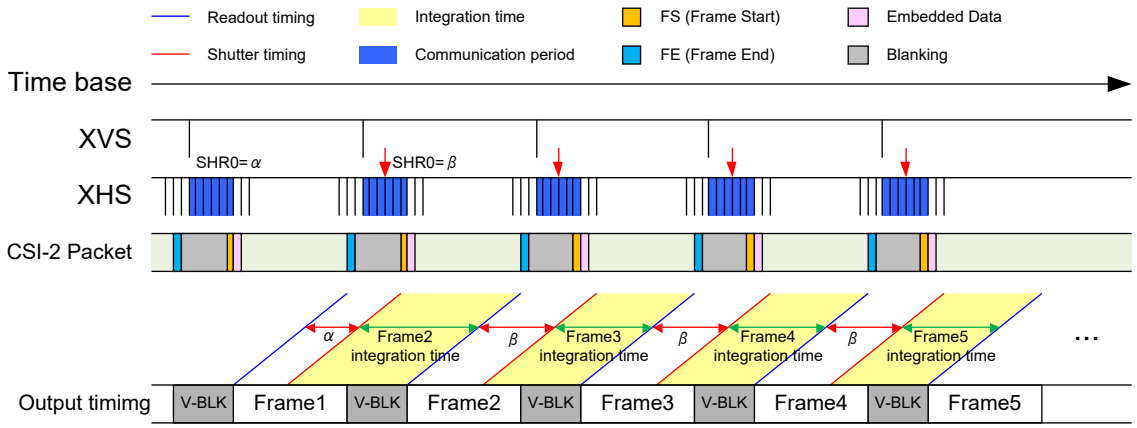


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval.
When the sensor is operating in master mode, it is done by designating a larger register VMAX [19:0] value compared to normal operation. When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

Although the maximum value of long exposure operation changes in each modes, the maximum of long time exposure is approximately 1 s.
When set to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed during long exposure operation.

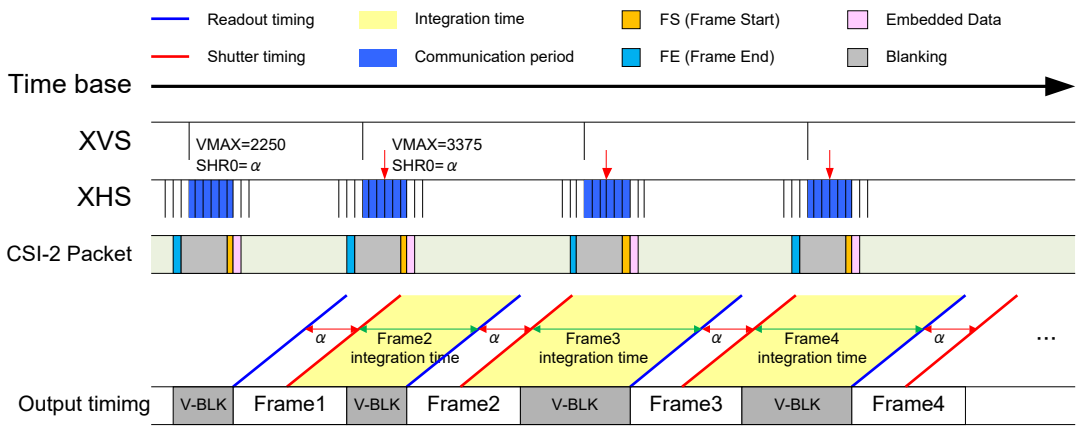


Image Drawing of Long Integration Time Control by Adjusting the Frame Period

Example of Integration Time Settings

The example of register setting for controlling the storage time is shown below.

Example of Integration Time Settings

Operation	Sensor setting (register)		Integration time
	VMAX*	SHR0**	
All-pixel scan mode	2250	2248	2H
		⋮	⋮
		2N	(2250 - 2N) H
		⋮	⋮
		6	2244H

* In sensor master mode. In slave mode, the interval is the same as XVS input.
** The SHR0 setting value (N) is set between “6” and “the VMAX value (M) – 2”.

Signal Output
CSI-2 output

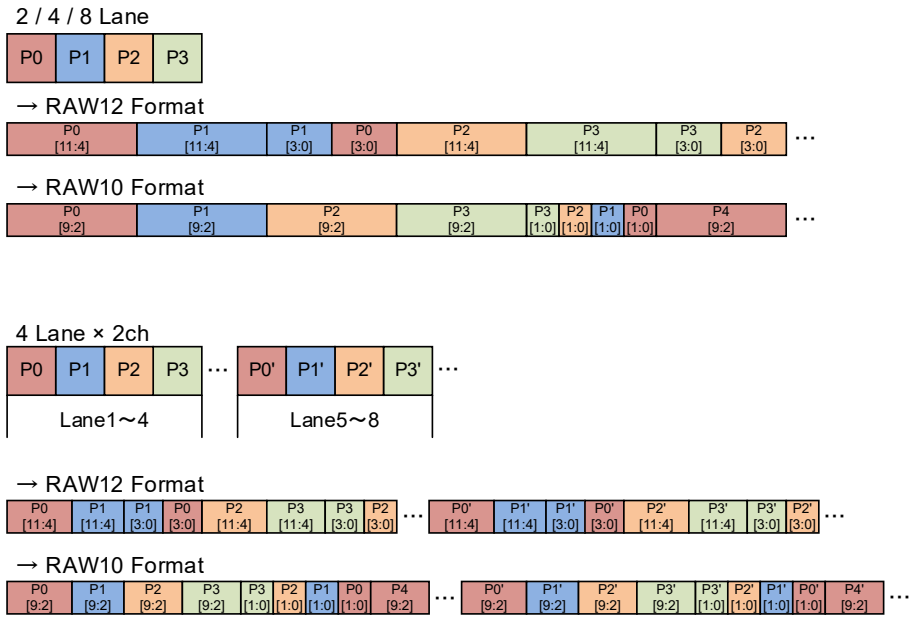
The output formats of this sensor support the following modes.

CSI-2 serial 2 Lane / 4 Lane / 8Lane / 4Lane × 2ch, RAW10 / RAW12

The 2 Lane / 4 Lane / 8 Lane / 4 Lane × 2ch serial signal output method using this sensor is described below.
Complied with the CSI-2, data is output using 2 Lane / 4 Lane. The image data is output from the CSI-2 output pin.
The DMO1P / DMO1N are called the Lane1 data signal, the DMO2P / DMO2N are called the Lane2 data signal, the DMO3P / DMO3N are called the Lane3 data signal, the DMO4P / DMO4N are called the Lane4 data signal, the DMO5P / DMO5N are called the Lane5 data signal, the DMO6P / DMO6N are called the Lane7 data signal, the DMO7P / DMO7N are called the Lane7 data signal, the DMO8P / DMO8N are called the Lane8 data signal.
In addition, the clock signals are output from DCK1P / DCK1N / DCK2P / DCK2N of the CSI-2 pins.
About 2 Lane / 4 Lane / 8 Lane , Use a clock signal of DCK1P / DCK1N.
About 4 Lane × 2ch, as for Lane 1-4, DCK1P / DCK1N, Lane 5-8 use a clock signal of DCK2P / DCK2N.
In 2 Lane mode, data is output from Lane1 and Lane2.
In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4.
In 8 Lane mode, data is output from Lane1, Lane2, Lane3, Lane4, Lane5, Lane6, Lane7, Lane8.
In 4 Lane × 2ch mode, data is output divide a horizontal direction from side to side, and the left side outputs the Lane1,2,3,4 right side from Lane5,6,7,8.
The bit rate maximum value is 1440 Mbps / Lane in 4Lane × 2ch mode, 1188 Mbps / Lane in 8Lane mode, 1782 Mbps / Lane in 4 Lane mode and 1782 Mbps / Lane in 2 Lane mode.
The select of RAW10 / RAW12 is set by the register: MDBIT [0]. The number of output lanes is set by the register: LANEMODE [2:0]. Unused lanes output signals conformed to MIPI standard.

Register	Register details		Initial value	Setting value
	Address	bit		
MDBIT	3032h	[0]	1h	0h: RAW10 1h: RAW12
LANEMODE [2:0]	3D01h	[2:0]	3h	1h: 2lane 3h: 4lane 6h: 4lane × 2ch 7h: 8lane

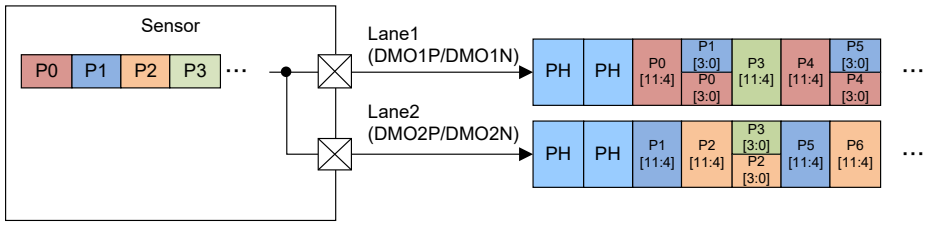
The formats of RAW12 and RAW10 are shown below.



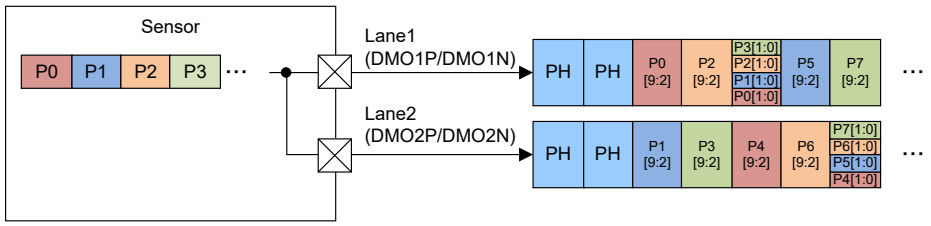
The Example of Format of RAW12 / RAW10

The each formal of 2 Lane, 4 Lane, 4Lane × 2ch and 8 Lane are shown below.

a) 2 Lane-RAW12

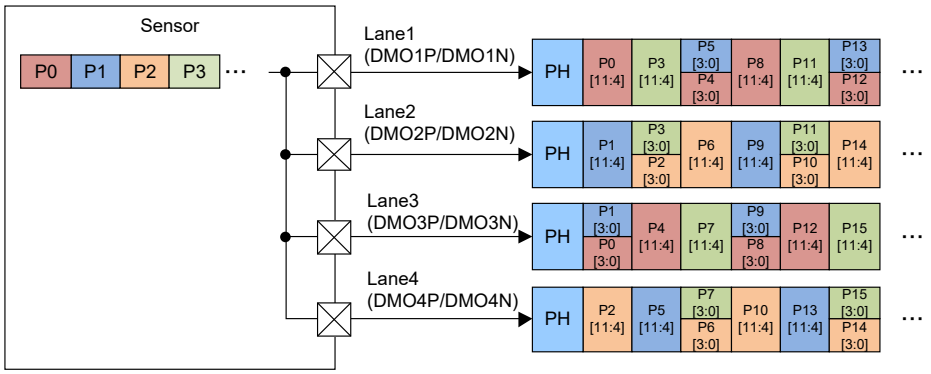


b) 2 Lane-RAW10

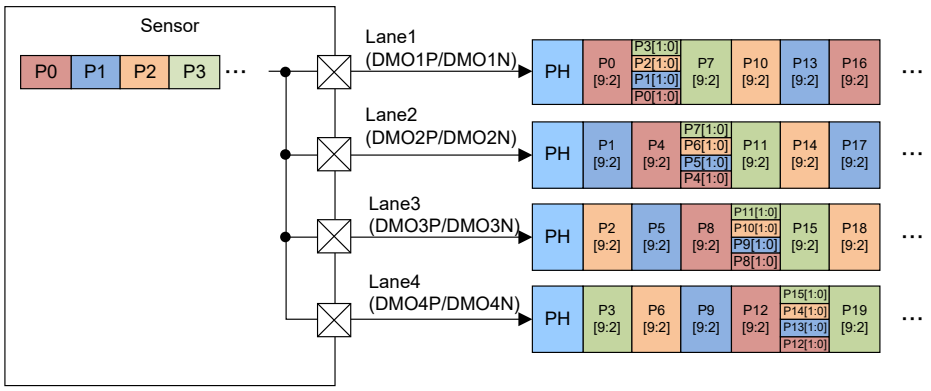


2 Lane Output Format

c) 4 Lane-RAW12

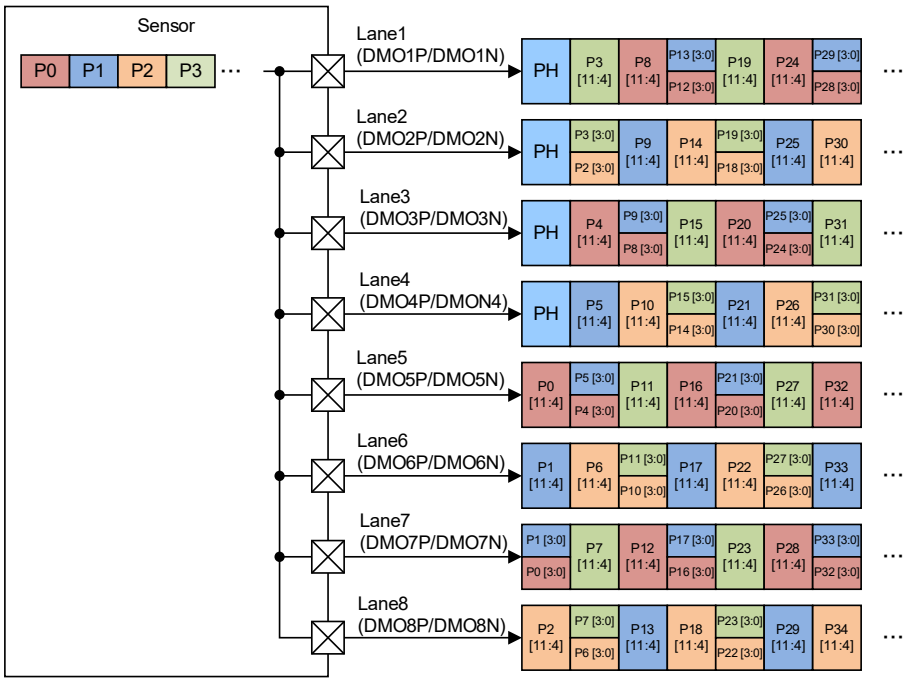


d) 4 Lane-RAW10

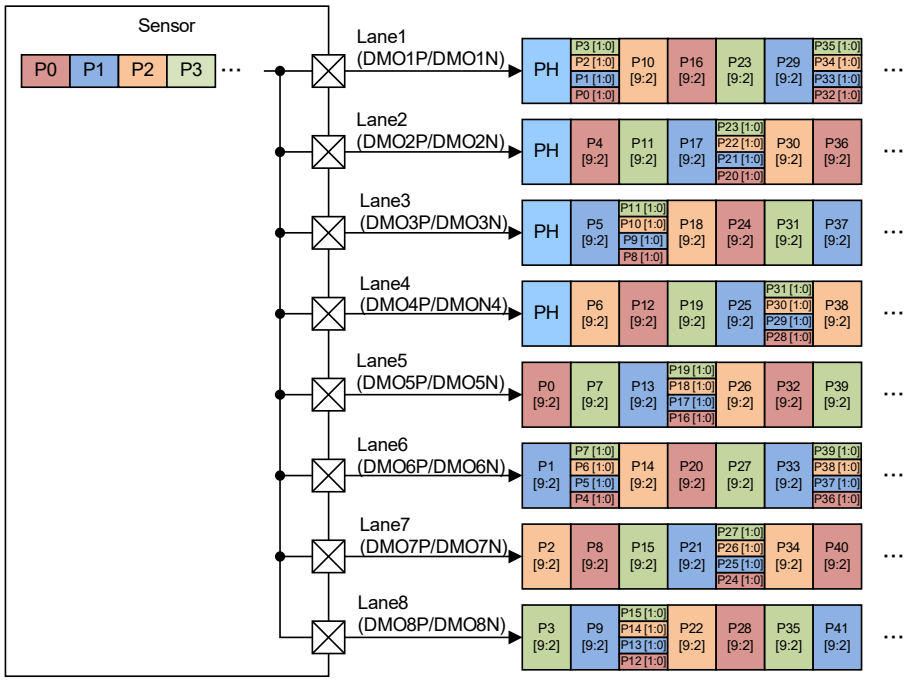


4 Lane Output Format

e) 8 Lane-RAW12

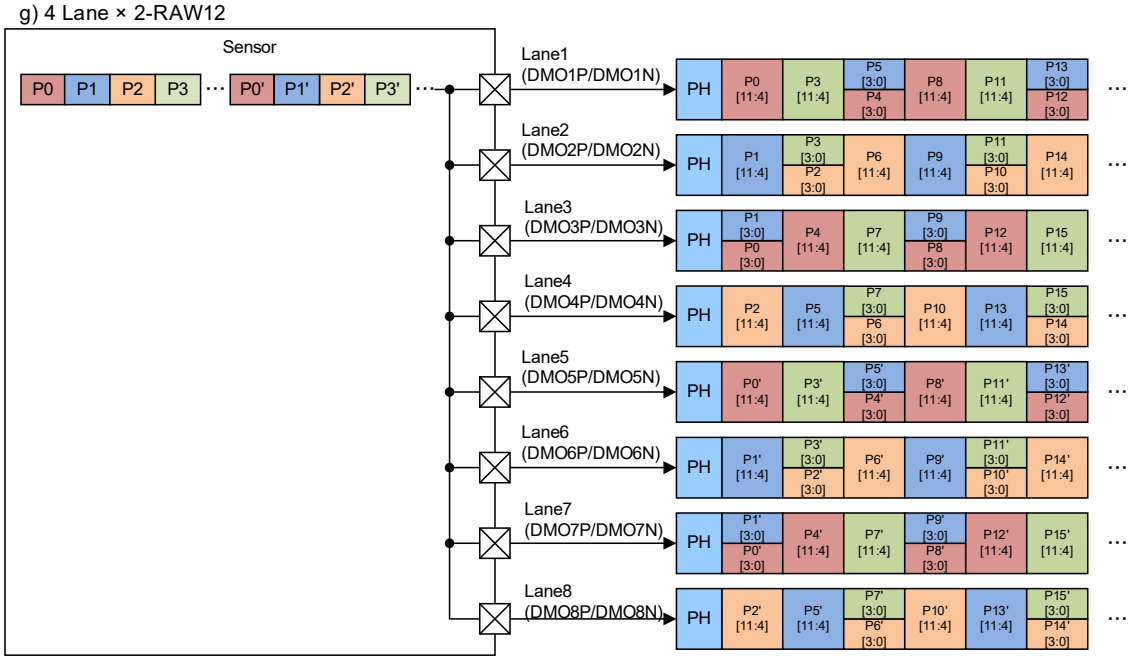


f) 8 Lane-RAW10

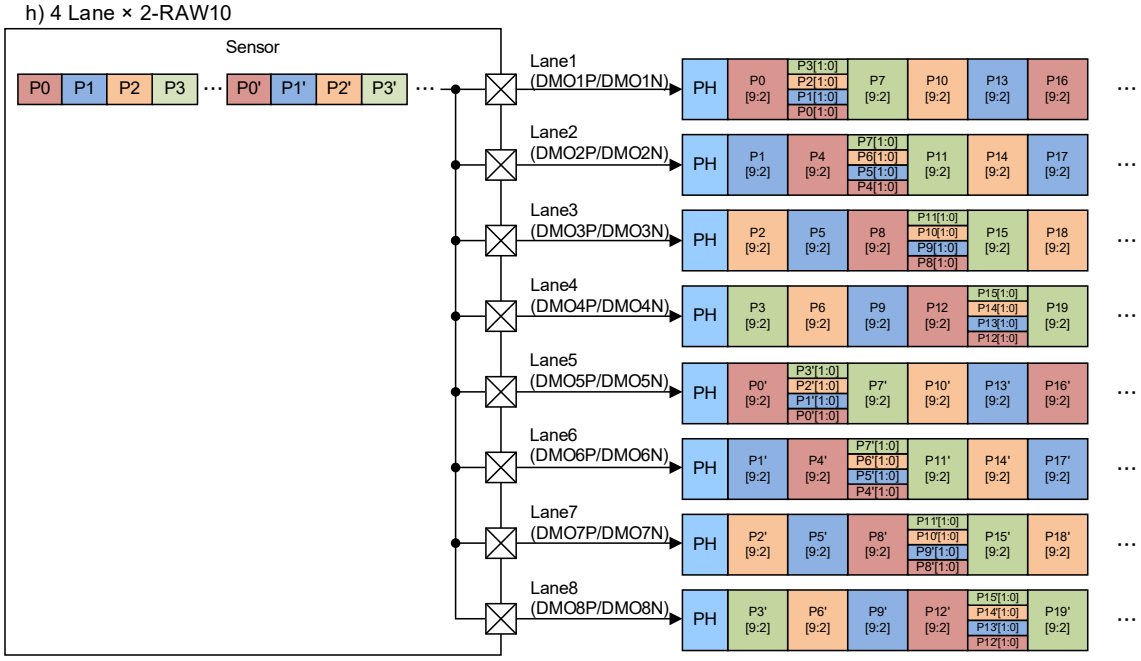


8 Lane Output Format

g) 4 Lane × 2-RAW12



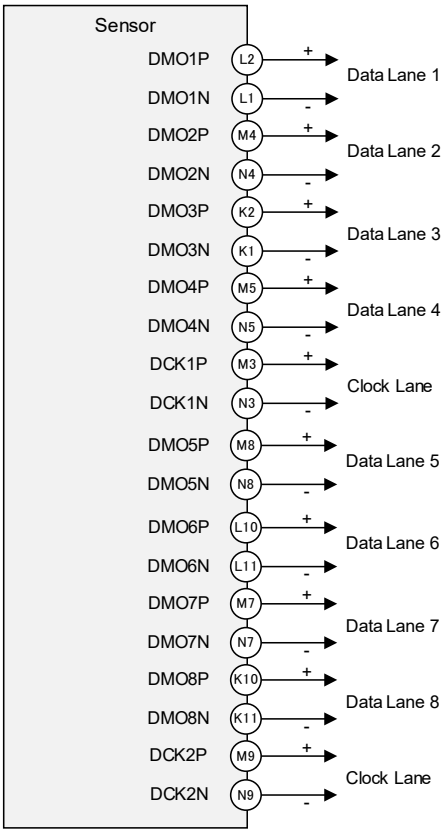
h) 4 Lane × 2-RAW10



4 Lane × 2ch Output Format

MIPI Transmitter

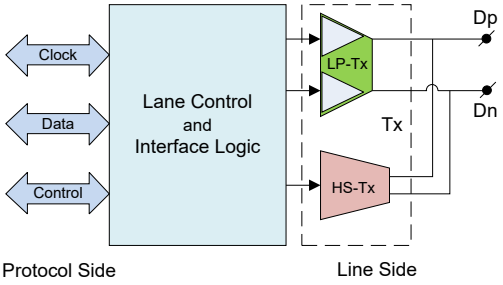
Output pins (DMO1P, DMO1N, DMO2P, DMO2N, DMO3P, DMO3N, DMO4P, DMO4N, DMO5P, DMO5N, DMO6P, DMO6N, DMO7P, DMO7N, DMO8P, DMO8N,DCK1P, DCK1N, DCK2P, DCK2N) are described in this section.



Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard
・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.20.00
・MIPI Alliance Specification for D-PHY Version 1.20.00

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver. The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane is as follows.
About 2 Lane and 4 Lane, 1782 Mbps / Lane.
About 8 Lane and 4 Lane × 2ch, 1440 Mbps / Lane.



Universal Lane Module Functions

Number of Internal A/D Conversion Bits Setting

The number of internal A/D conversion bits can be selected from 10 bits or 12 bits by the register ADBIT. See the section of “Operating Modes” for the correspondence with each mode.

List of Bit Width Selection

Register	Register details		Initial value	Setting value
	Address	bit		
ADBIT	3031h	[0]	1h	0: 10 bit 1: 12 bit

Output Signal Range

In CSI-2 output mode, the sensor output has either a 10 bit or 12 bit gradation, and the maximum output value is the 3FFh value (10 bit output) and the FFFh one (12 bit output).
The output range for each output gradation is shown in the table below.

Output Gradation and Output Range (CSI-2 Output)

Output gradation	Output value	
	Min.	Max.
10 bit	000h	3FFh
12 bit	000h	FFFh

INCK Setting

The available operation mode varies according to INCK frequency. Input either 27 MHz, 37.125 MHz or 74.25 MHz for INCK frequency. The INCK setting register and the list of INCK setting are shown in the table below.

In the MIPI Alliance Specification for D-PHY Version 1.2,
when operating above 1500 Mbps, an initial deskew sequence shall be transmitted before High-Speed Data Transmission. When operating at or below 1500 Mbps, the transmission of the initial deskew sequence is optional. When operating at or above 1440 Mbps, this Sensor transmits the initial deskew burst.

INCK Setting Register

Register	Register details		Initial value	INCK [MHz]		
	Address	Bit		27	37.125	74.25
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Ch	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
EFWAIT_TIME	300Bh	[7:4]	Ah	4h	5h	Ah
INCKSEL1	3114h	[1:0]	3h	2h	2h	3h
INCKSEL4	3804h	[1:0]	3h	2h	2h	3h
INCKSEL5	3807h	[7:0]	60h	84h	60h	60h
TXCLKESC_FREQ	3D05-04h	[15:0]	1290h	06C0h	0948h	1290h

Register	Register details		Initial value	Data Rate [Mbps/Lane]	
	Address	Bit		594 to 891	1188 to 1782
INCKSEL2	3119h	[1:0]	0h	1h	0h

Register	Register details		Initial value	INCK [MHz]		
	Address	Bit		27	37.125	74.25
INCKSEL3	311D-1Ch	[8:0]	0C0h	*1	*2	*2

*1: About 1188 to 1782 [Mbps/Lane]
INCKESEL3 = Data Rate[Mbps/Lane] / 6.75

About 594 to 891 [Mbps/Lane]
INCKESEL3 = Data Rate[Mbps/Lane] × 2 / 6.75

*2: About 1188 to 1782 [Mbps/Lane]
INCKESEL3 = Data Rate[Mbps/Lane] / 9.28125

About 594 to 891 [Mbps/Lane]
INCKESEL3 = Data Rate[Mbps/Lane] × 2 / 9.28125

*Rounded down decimal point.

Register	Register details		Initial value	Data Rate [Mbps/Lane]	
	Address	Bit		594 to 891, 1188 to 1439	1440 to 1782
INCKSEL6	3D0Ch	[0]	1h	0h	1h

Global Timing setting

The table below shows the setting value of Global Timing available with about change “Data Rate”.

Address	Register name	Data Rate [Mbps/Lane]				
		594 to 667	668 to 725	726 to 799	800 to 857	858 to 891
3D18h to 3D19h	TCLKPOST	0067h	006Fh	006Fh	0077h	007Fh
3D1Ah to 3D1Bh	TCLKPREPARE	0027h	002Fh	002Fh	0037h	0037h
3D1Ch to 3D1Dh	TCLKTRAIL	0027h	002Fh	002Fh	0037h	0037h
3D1Eh to 3D1Fh	TCLKZERO	00B7h	00BFh	00D7h	00DFh	00F7h
3D20h to 3D21h	THSPREPARE	002Fh	002Fh	0037h	0037h	003Fh
3D22h to 3D23h	THSZERO	004Fh	0057h	005Fh	0067h	006Fh
3D24h to 3D25h	THSTRAIL	002Fh	002Fh	0037h	0037h	003Fh
3D26h to 3D27h	THSEXIT	0047h	004Fh	0057h	0057h	005Fh
3D28h to 3D29h	TLPX	0027h	0027h	002Fh	002Fh	002Fh

Address	Register name	Data Rate [Mbps/Lane]				
		1188 to 1197	1198 to 1255	1256 to 1327	1328 to 1387	1388 to 1459
3D18h to 3D19h	TCLKPOST	008Fh	0097h	0097h	009Fh	009Fh
3D1Ah to 3D1Bh	TCLKPREPARE	004Fh	004Fh	004Fh	0057h	0057h
3D1Ch to 3D1Dh	TCLKTRAIL	0047h	004Fh	004Fh	0057h	0057h
3D1Eh to 3D1Fh	TCLKZERO	0137h	014Fh	015Fh	016Fh	0187h
3D20h to 3D21h	THSPREPARE	004Fh	004Fh	0057h	0057h	005Fh
3D22h to 3D23h	THSZERO	0087h	0097h	0097h	009Fh	00A7h
3D24h to 3D25h	THSTRAIL	004Fh	004Fh	0057h	0057h	005Fh
3D26h to 3D27h	THSEXIT	007Fh	0087h	008Fh	008Fh	0097h
3D28h to 3D29h	TLPX	003Fh	003Fh	0047h	0047h	004Fh

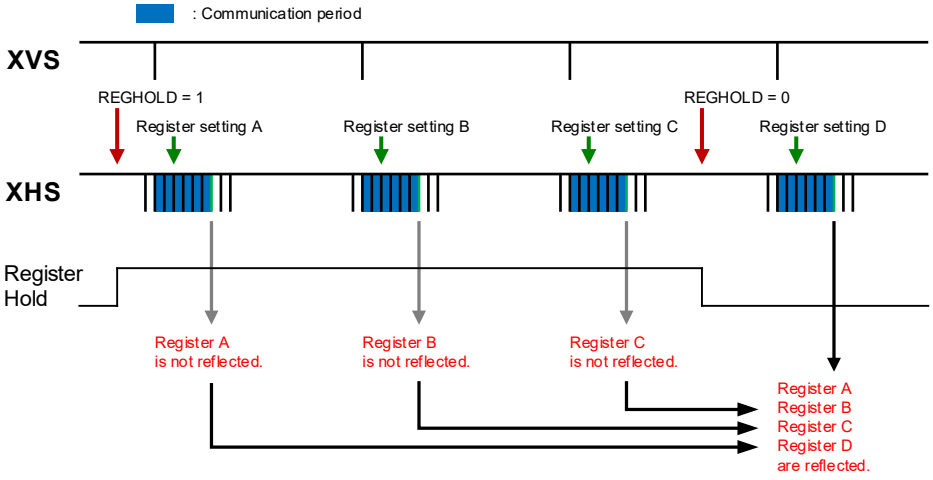
Address	Register name	Data Rate [Mbps/Lane]				
		1460 to 1519	1520 to 1591	1592 to 1651	1652 to 1723	1724 to 1782
3D18h to 3D19h	TCLKPOST	00A7h	00AFh	00AFh	00B7h	00B7h
3D1Ah to 3D1Bh	TCLKPREPARE	0057h	005Fh	005Fh	0067h	0067h
3D1Ch to 3D1Dh	TCLKTRAIL	005Fh	005Fh	0067h	0067h	006Fh
3D1Eh to 3D1Fh	TCLKZERO	0197h	01A7h	01BFh	01CFh	01DFh
3D20h to 3D21h	THSPREPARE	005Fh	0067h	0067h	006Fh	006Fh
3D22h to 3D23h	THSZERO	00AFh	00B7h	00BFh	00BFh	00CFh
3D24h to 3D25h	THSTRAIL	005Fh	0067h	0067h	006Fh	006Fh
3D26h to 3D27h	THSEXIT	009Fh	00A7h	00AFh	00B7h	00B7h
3D28h to 3D29h	TLPX	004Fh	0057h	0057h	0057h	005Fh

Register Hold Setting

V reflected register setting can be transmitted with divided to several frames and it can be reflected globally at acertain frame by the register REGHOLD. Setting REGHOLD = 1 prevents the registers that set thereafter from being reflected at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the desired frame to reflect the register.

Register Hold Setting Register

Register	Register details		Initial value	Setting value
	Address	bit		
REGHOLD	3001h	[0]	0h	0: Invalid 1: Valid (Register hold)



Register Hold Setting

Mode Transitions

The Mode transition between operations is shown below. These examples shown in case that setting is completed within one communication timing.

List of Mode Transition

Transition			State
Horizontal direction normal	→	Horizontal direction inverted	Via the Standby state is unnecessary.
Horizontal direction inverted	→	Horizontal direction normal	
All-pixel scan mode	→	Window cropping mode	Via the Standby state is unnecessary. One invalid frame is generated.
Window cropping mode	→	All-pixel scan mode	
Vertical direction normal	→	Vertical direction inverted	
Vertical direction inverted	→	Vertical direction normal	
Vertical direction line number change (Master mode : VMAX change, Slave mode : XVS interval change)			
Horizontal direction 1H period change (Master mode : HMAX change, Slave mode : XHS interval change)			
- Transition between modes other than above - Change the input frequency of INCK *1 - Change the register setting noted “S” in the reflection timing column of the Register Map.			Via the standby state is necessary.

*1 When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

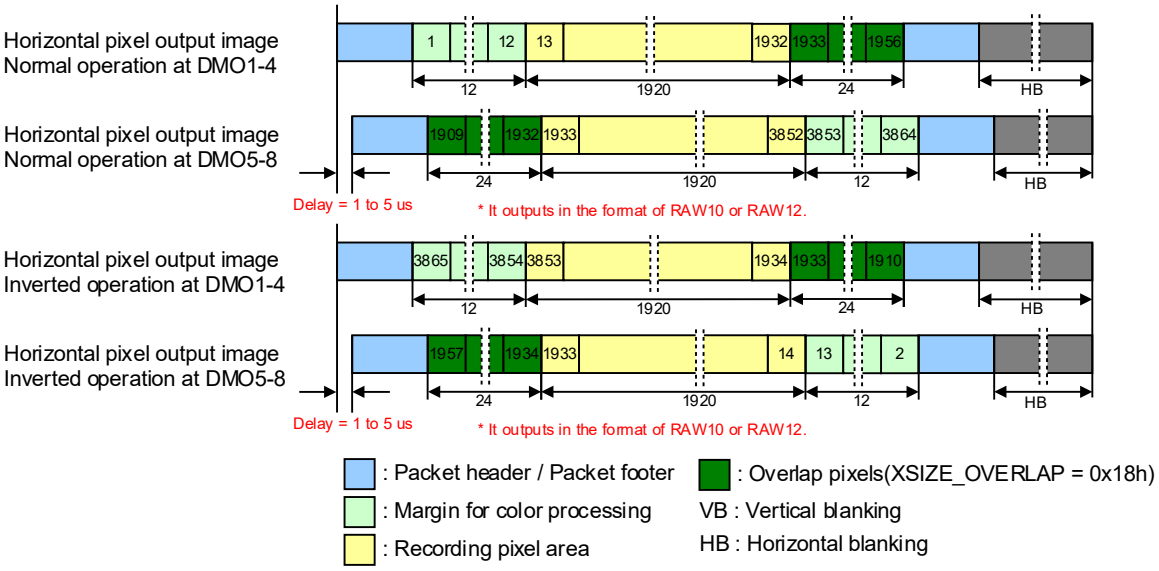
XSIZE_OVERLAP Setting

The XSIZE_OVERLAP register can be duplicated for H pixel several minutes when set XSIZE_OVERLAP[10:0] and can output the frame of right and left.

Use with values shown below is recommended.
Effective only in “4Lane × 2ch”.

XSIZE_OVERLAP Register

Register	Register details		Initial value	Setting value
	Address	Bit		
XSIZE_OVERLAP[10:0]	3040h	[7:0]	000h	000h to 3F0h Multiples of 12 (MAX 1008d(3F0h)) Smaller than PIX_HWIDTH
	3041h	[2:0]		



The Example of Format of XSIZE_OVERLAP

Other Function

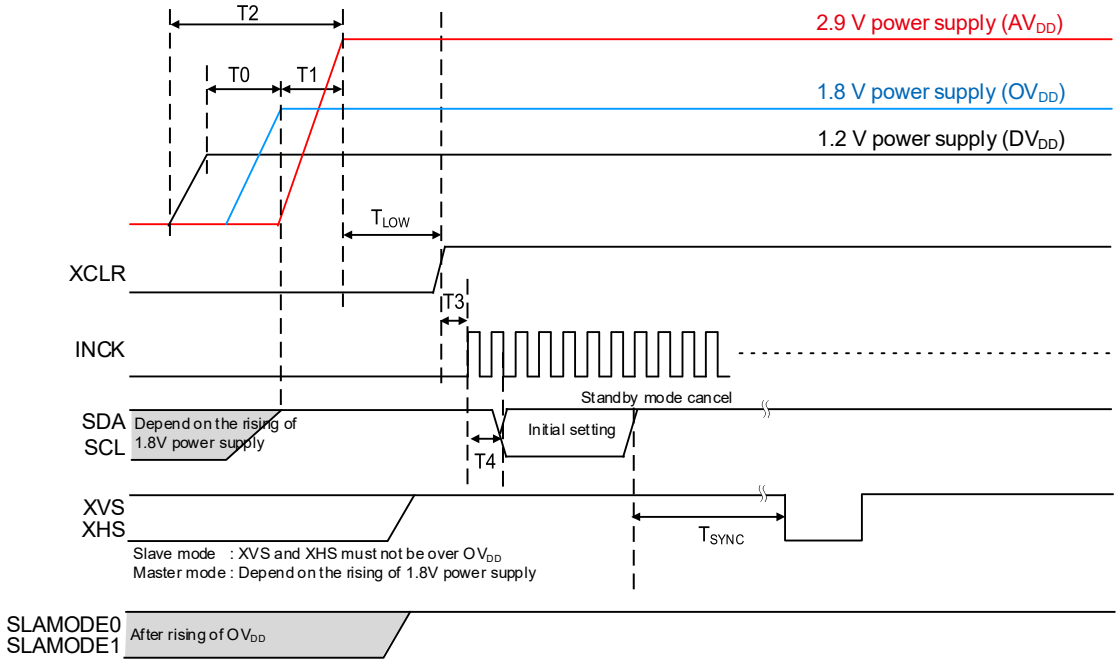
This sensor has the function as below. About detail, refer to each application note.

- Digital overlap HDR (2 / 3 frame)
- Multiple exposure HDR (2 / 4 frame)
- Additional Function of Synchronizing Sensors

Power-on and Power-off Sequence

Power-on sequence

1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 2.9 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
3. The system clear is applied by setting XCLR to High level. The maser clock input after setting the XCLR pin to High level.
4. Make the sensor setting by register communication after the system clear.

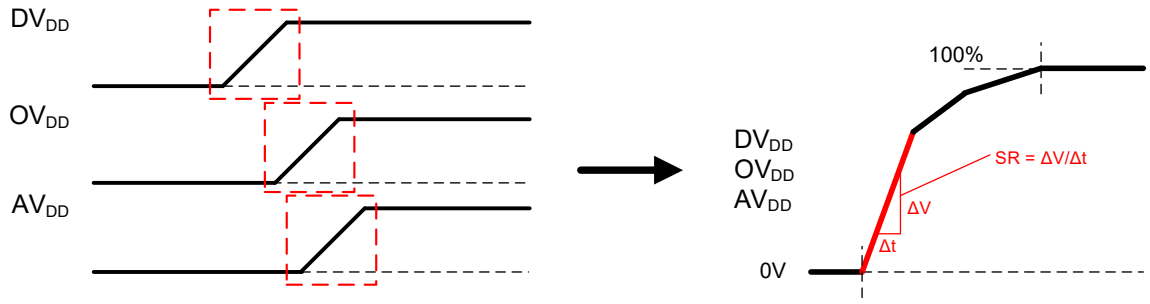


Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.2 V power supply rising → 1.8 V power supply rising	T0	0	—	ns
1.8 V power supply rising → 2.9 V power supply rising	T1	0	—	ns
Rising time of all power supply	T2	—	200	ms
2.9 V power supply rising → Clear OFF	T_{LOW}	500	—	ns
Clear OFF → INCK rising	T3	1	—	μs
Clear OFF → Communication start	T4	20	—	μs
Standby OFF (communication) → External input XHS, XVS (slave mode only)	T_{SYNC}	24	—	ms

Slew Rate Limitation of Power-on Sequence

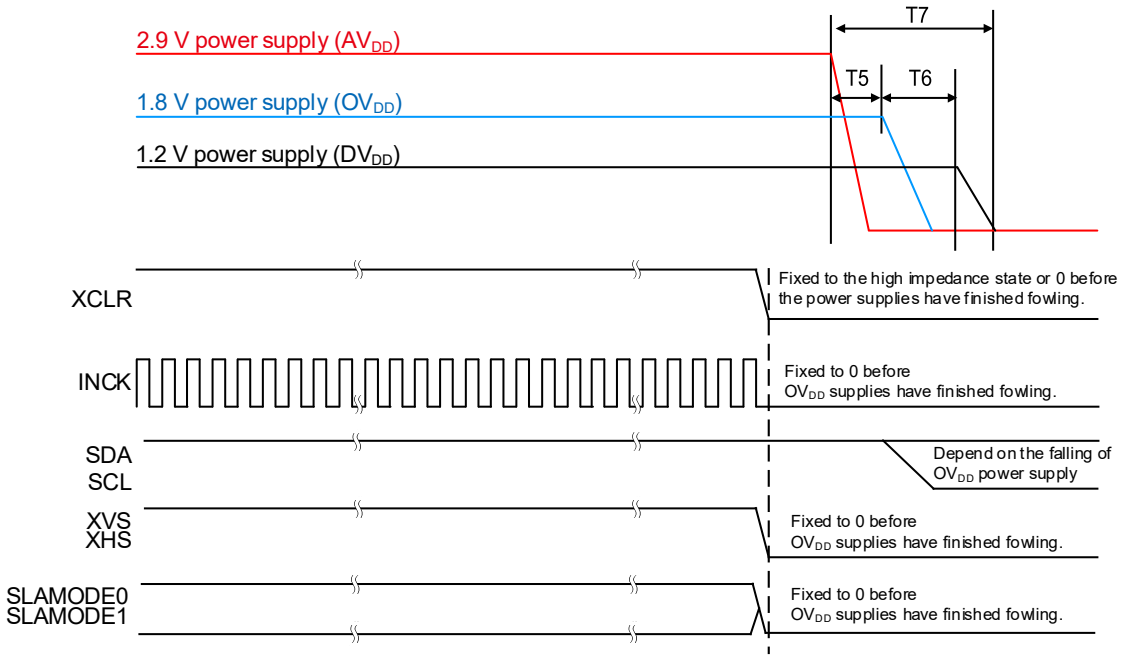
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	DV_{DD} (1.2 V)	—	25	mV/μs	
		OV_{DD} (1.8 V)	—	25	mV/μs	
		AV_{DD} (2.9 V)	—	25	mV/μs	

Power-off sequence

Turn Off the power supplies so that the power supplies fall in order of 2.9 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should be falling within 200 ms. Set each digital input pin (INCK, SDA, SCL, XCLR, XVS, XHS, SLAMODE0, SLAMODE1) to 0 V before the 1.8 V power supply (OV_{DD}) falls.



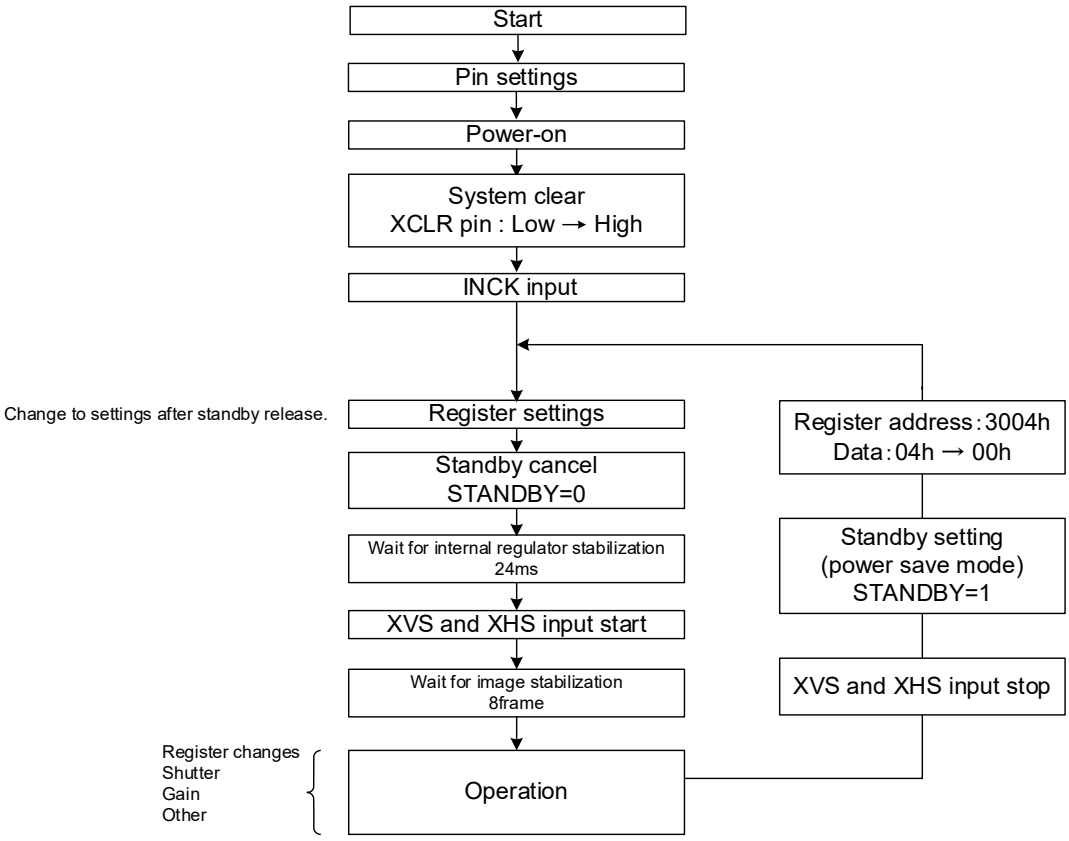
Power-off Sequence

Item	Symbol	Min.	Max.	Unit
2.9 V power shut down → 1.8 V power shut down	T5	0	—	ns
1.8 V power shut down → 1.2 V power shut down	T6	0	—	ns
Shut down time of all power supply	T7	—	200	ms

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

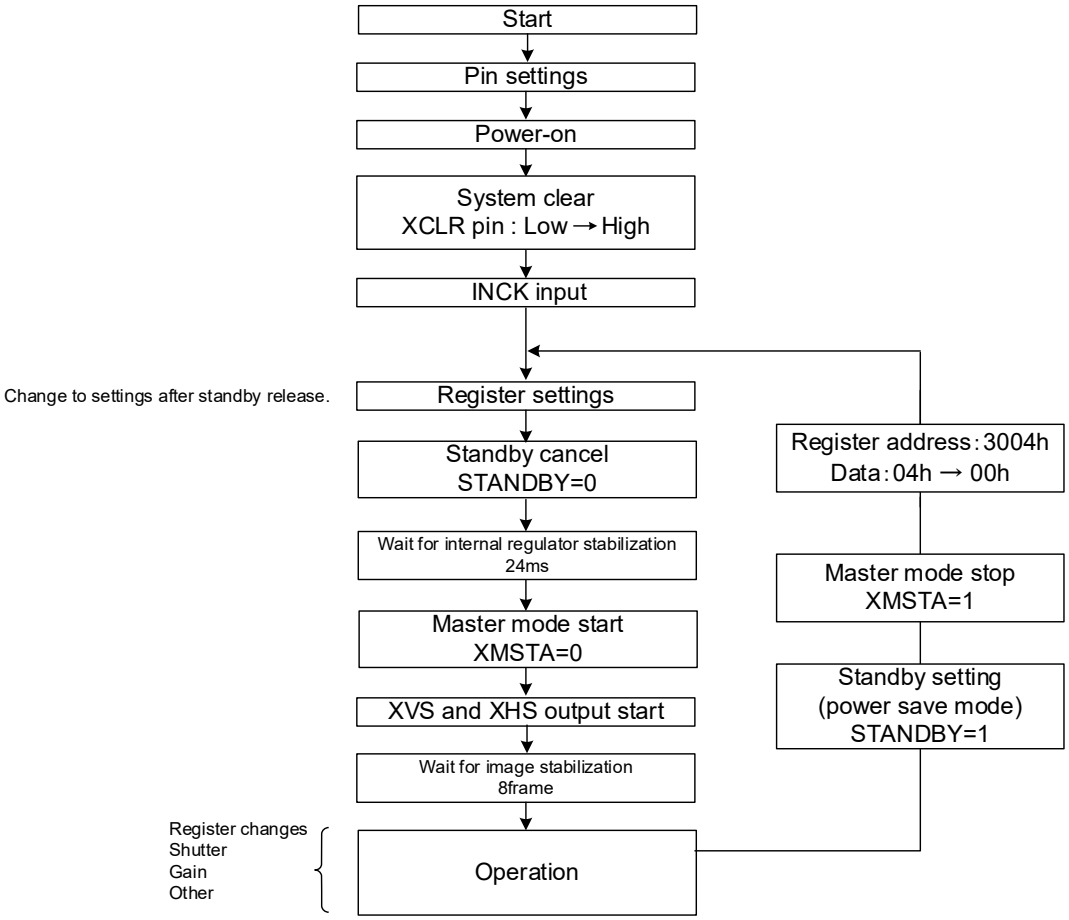
The figure below shows operating flow in sensor slave mode.
For details of "Power-on" to "Reset cancel", see the item of "Power-on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

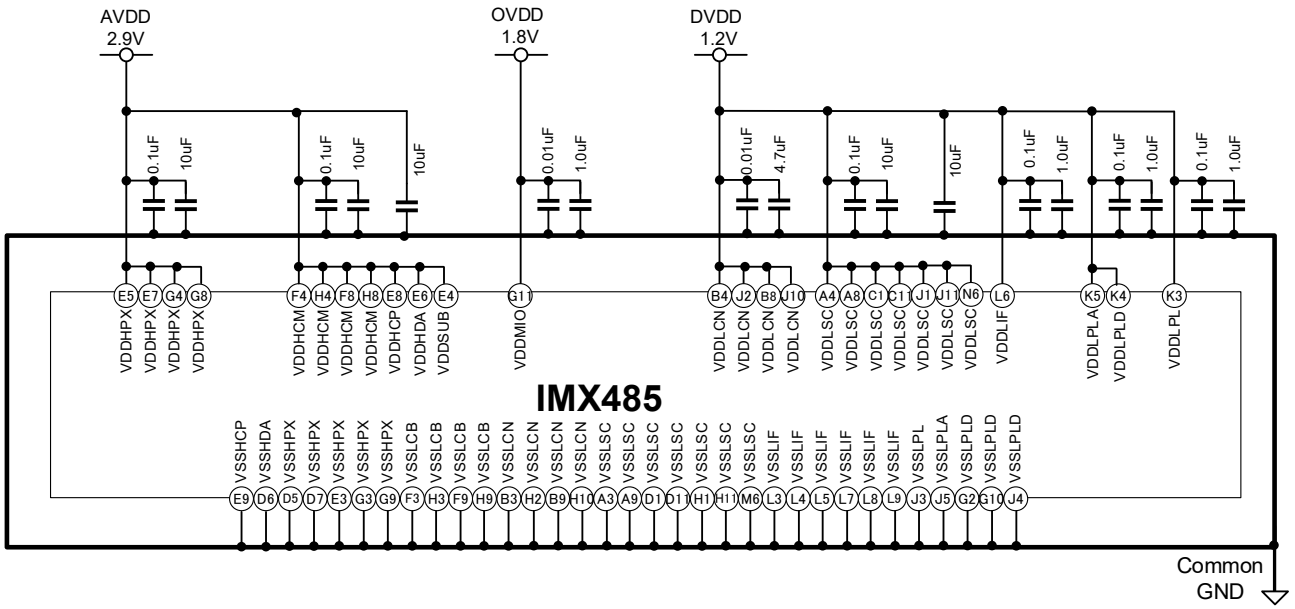
Setting Flow in Sensor Master Mode

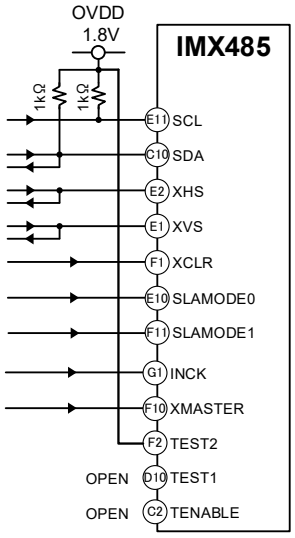
The figure below shows operating flow in sensor master mode.
For details of "Power-on" to "Reset cancel", see the item of "Power on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
In master mode, “Master mode start” by setting register XMSTA to “0” after “Waiting for internal regulator stabilization”
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".

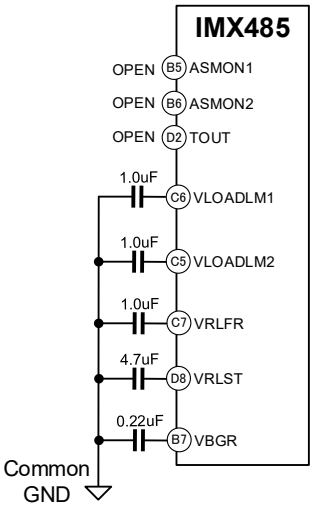


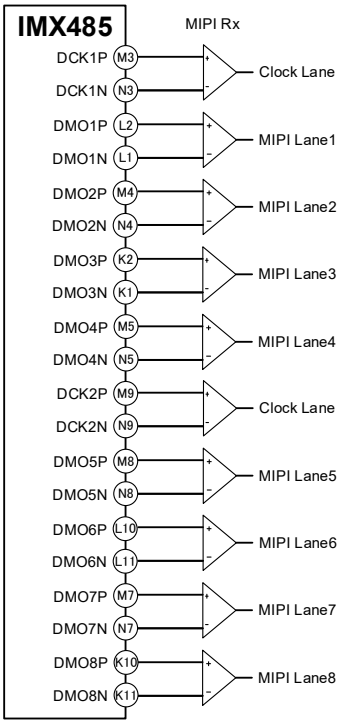
Sensor Setting Flow (Sensor Master Mode)

Peripheral Circuit









Application circuits shown are typical examples illustrating the operation of the devices.
Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

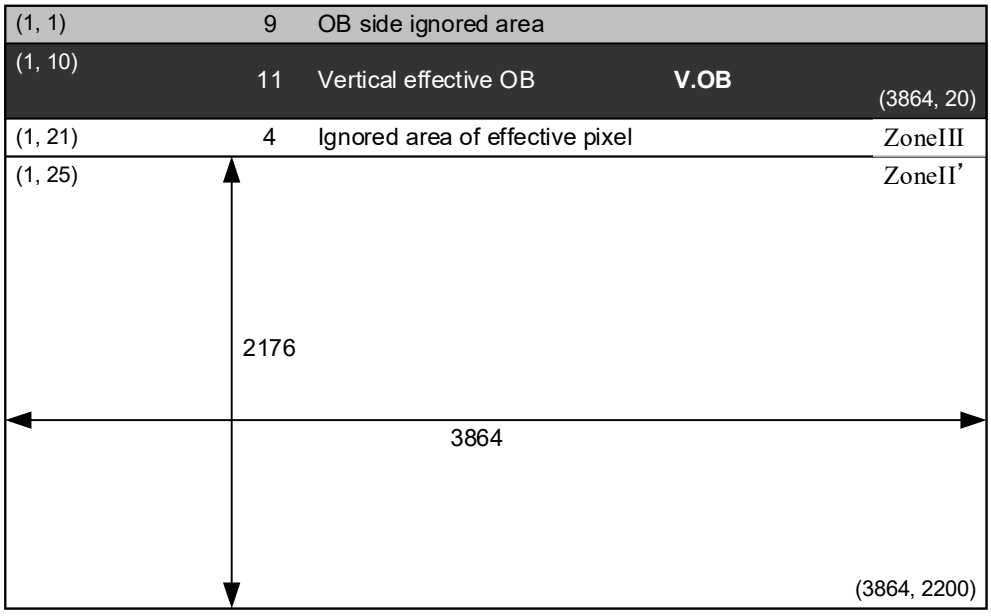
Spot Pixel Specifications

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, 30 frame/s, Gain: 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30 % ≤ D	60	No evaluation criteria applied			1	
White pixels in the dark	5.6 mV ≤ D	800		No evaluation criteria applied		2	1/30 s storage
Black pixels at signal saturated	D ≤ 668 mV	0	No evaluation criteria applied			3	

Note) 1. Zone is specified based on all-pixel drive mode
2. D Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	73 pcs
10.0 mV or higher	41 pcs
24.0 mV or higher	17 pcs
50.0 mV or higher	8 pcs
72.0 mV or higher	6 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

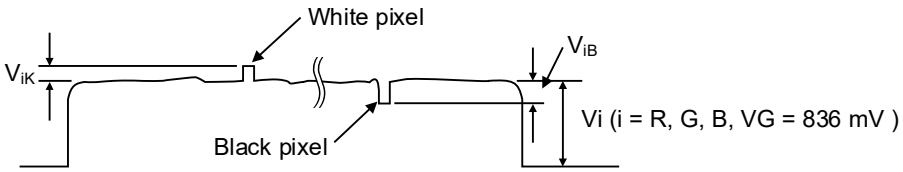
Material_No.03-0.0.10

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 836 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

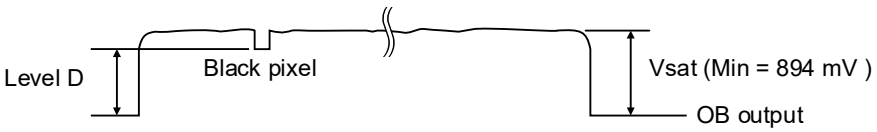
   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



Signal output waveform of R / G / B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

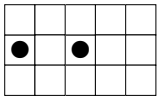
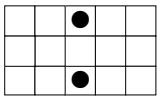


Signal output waveform of R/G/B channel

Spot Pixel Pattern Specification

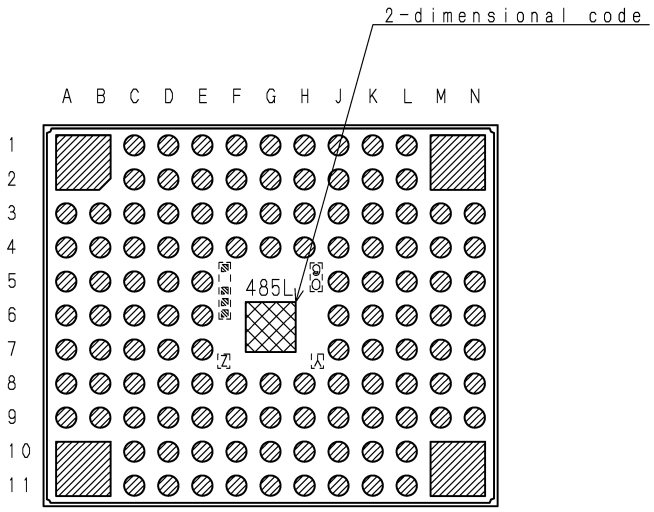
White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

No.	Pattern (R G / G B)	White pixel Black pixel Bright pixel
1		Rejected
2		Rejected

Note) 1.”●” shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated “Rejected” is selected and removed.
3. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Marking



Note:Following characters enter into "Y", and"Z". (No Au coat)

Y:In English upper case character, One character
Z:Number, single number

DRAWING No. AM-B485LQJ(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

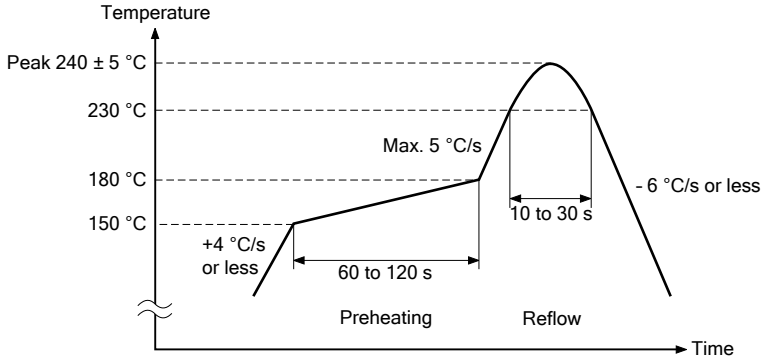
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing. Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass. (The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

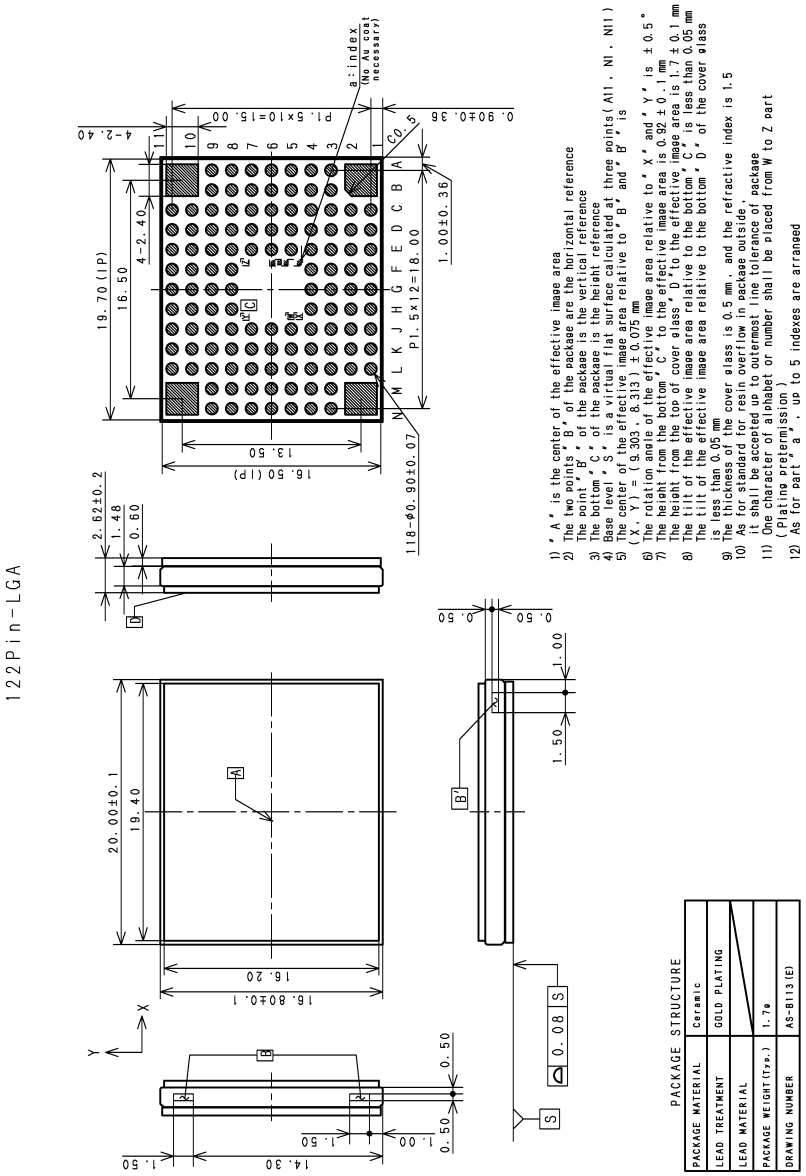
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

(6) Please perform the tilt adjustment for the optical axis in your company as required.

Package Outline

(Unit: mm)



List of Trademark Logos and Definition Statements

STARVIS

* STARVIS is a trademark of Sony Corporation. The STARVIS is back-illuminated pixel technology used in CMOS image sensors for surveillance camera applications. It features a sensitivity of 2000 mV or more per 1 μm^2 (color product, when imaging with a 706 cd/m^2 light source, F5.6 in 1 s accumulation equivalent), and realizes high picture quality in the visible-light and near infrared light regions.

Revision History

Date of change	Ver.	Page	Contain of Change
2019/3/27	0.1	-	First Edition
2019/5/24	0.2	10	Correction: Pin Configuration D6 Pin VSSHPX → VSSHDA
		15	Correction: Operating current. Stanby 1.2V → 1.3V
		24	Delete: Measurement Conditions which is taken as the value of the …
		25	Correction: 8 Conversion efficiency ratio LCH → LCG
		27	Correction: Register Communication Timing, description
		42, 43, 44	Delete: Register address 34C6h, 34C7h Correction: Register address 3366h, 34CEh, 34CFh Add: Register address 3416h, 35C0h, 35C2h, 3888h, 388Ch, 39A2h-39A7h, 39D2h-39D3h, 39D8h-39DBh, 39E0h-39E3h, 39E8h-39EBh, 39F2h-39F3h, 3A00h-3A03h, 3A18h-3A19h, 3A2Ah-3A2Bh, 3A30h-3A33h, 3A36h-3A37h, 3A3Eh-3A47h, 3A4Eh, 3A50h-3A53h
		55	Correction: Drive Timing Chart for All pixel mode
		56	Correction: Drive Timing Chart for All pixel mode
		61	Correction: Drive Timing Chart for Horizontal /Vertical 2/2-line binning mode
		62	Correction: Drive Timing Chart for Horizontal /Vertical 2/2-line binning mode
		63	Correction: Image Drawing of Window Cropping Mode in Horizontal/Vertical, normal/inverted direction
		64	Correction: Description of the explanation of the following register PIX_HST, PIX_VST, PIX_VWIDTH
		80	Correction: Relationship between Pin Name and MIPI Output Lane DMO1P = L1 Pin → DMO1P = L2 Pin DMO1N = L2 Pin → DMO1N = L1 Pin DCK1M → DCK1N DCK2M → DCK2N
		81	Correction: Output Signal Range Deleted “but output is not performed over the full range,”
		84	Correction: Register Hold Setting Part of sentence
		92	Correction: Peripheal Circuit F2 Pin XHS → E2 Pin XHS
		97	Update: Marking
		100	Update: Package Outline

Date of change	Ver.	Page	Contain of Change
2019/6/28	0.3	1	Update: TBD
		23	Correction: Image Sensor Characteristics(TBD)
		37	Update: XSIZE_OVERLAP Value
		39	Update:TBD
		42	Add: 3260h, 3262h, 3278h, 3324h, 3432h
		43	Add: 35ACh
		44	Correction: 3A18h
		62	Correction: Pixel Array Image Drawing in Horizontal /Vertical 2/2-line binning mode(4 Lane × 2ch) Horizontal Effeective margin for color processing “12” → ”6”
		65	Correction: Restrictions on Window cropping mode (PIX_VWIDTH / 2) → PIX_VWITDH
		69	Update:TBD
		76	Correction: CSI-2 output In 4 Lane × 2ch mode, data is split into two and outputs in Lane1,2,3,4 and Lane5,6,7,8. → In 4 Lane × 2ch mode, data is output divide a horizontal direction from side to side, and the left side outputs the Lane1,2,3,4 right side from Lane5,6,7,8.
		80	Update: TBD
		86	Update: XSIZE_OVERLAP Setting
		91, 92	Update: TBD
2019/7/12	0.4	11	Correct: Description of the ”I/O” column of “VRLFR” , ”VRLST” GND → O
		50	Delete: “SHR0” which is listed in “18 to 23” of the table
		63	Correction: Image Drawing of Window Cropping Mode in Horizontal/Vertical, normal/inverted direction
		94	Correct: Value of the V direction of the figure of “Zone Definition”

Date of change	Ver.	Page	Contain of Change
2019/9/13	E19903	1	Delete: Tentative
		7	Update: TBD
		10	Correction: 1.8 V / 1.2 V → 1.2 V / 1.8 V
		11 to 13	Correction: 1.2 V GND → 1.2 V / 1.8 V GND
		15	Update: TBD
		22	Update: Spectral Sensitivity Characteristics
		23	Update: TBD
		25	Update: TBD
		36	Correction: FDG_SEL “ V → S ”
		43 to 44	Add: 359Eh, 3798h, 379Ah, 379Ch, 379Ch, 3914h, 3915h, 3916h, 3917h, 3918h, 3919h, 391Ah, 391Bh, 391Ch, 391Eh, 391Fh, 3920h, 3921h
		46 to 47	Add: 1 V period [XVS]
		50	Correction: EBD of Figure
		52	Add: Image Data Output Format
		53 to 60	Correction: 3200h to 36FFh → 3152h to 37FFh Add: 3888h → 3AFFh
		62	Add: Image Data Output Format
		63 to 66	Correction: 3200h to 36FFh → 3152h to 37FFh Add: 3888h → 3AFFh
		68	Update: TBD
		71	Update: TBD Correction: PIX_VWIDTH + 30 → PIX_VWIDTH + 70
		92	Update: TBD
		100	Update: TBD
		101	Update: TBD
		102	Update: TBD
		104	Update: Marking
		106	Update: TBD
		107	Update: Package Outline

Date of change	Ver.	Page	Contain of Change
2019/10/10	E19903A9X	36	Correction: FDG_SEL0 "S" → "V"
		46	Correction: Description Global timing setting → The value is set according to Data Rate Refer to "Global Timing setting"
		47	Correction: Operationg mode table Add: "Variable Data Rate" section.
		56 to 59	Correction: [frame/s] 90 → 90.1
		64 to 65	Correction: [frame/s] 90 → 90.1
		85	Correction: About 8 Lane, 1188 Mbps / Lane. About 4 Lane × 2ch, 1440 Mbps / Lane. → About 8 Lane and 4 Lane × 2ch, 1440 Mbps / Lane.
		87	Correction: INCK setting Table.
		88	Add: "Global Timing setting" section.
2019/11/5	E19903B9X	87	Correction: INCKSEL2 594 to 891 = 0h → 1h 1188 to 1782 = 1h → 0h
2020/3/27	E19903C03	1	Correction: Readout rate 10 bit 90 frame/s → 10 bit 90.1 frame/s Deleted: Recommended exit pupil distance at Features
		24	Deleted: (exit pupil distance – 30 mm)
		47	Correction: Variable Data Rate 1784 → 1782
		66	Correction: Pixel Array Image Drawing in Horizontal /Vertical 2/2-line binning mode (2,4,8 Lanes)
		67	Correction: Pixel Array Image Drawing in Horizontal /Vertical 2/2-line binning mode (4 Lane × 2ch)
		68	Correction: Image Drawing of Window Cropping Mode in Horizontal/Vertical, normal/inverted direction
		69	Correction: List of Setting Register